Energy Efficient power gated True Single-Phase-Clocked Flip-Flop With Redundant-Precharge-Free Operation

PROF.S.M.PRASAD

M. Tech student,Dept of ECE (VLSI), SVPCET, JNTUA University, Puttur,Andhra Pradesh,India

Dr.RAMACHANDRA C G, M.Tech

Associate Professor,Dept of ECE,SVPCET,JNTUA University,Puttur, Andhra Pradesh,India

ABSTRACT

This paper presents the design of a Novel power gated true single phase clocked Flipflop. Power optimization is a very crucial issue in low voltage applications. This paper presents a design of D-Flip flop circuit using header power gating technique for low power operation. The main aim of the design is to investigate the power dissipation for D Flipflop for the proposed design style. The proposed design is implemented in Tanner EDA. The simulation results show the there is a significant reduction in power consumption for this proposed cell with power gating.

Keywords: Power gating, D Flipflop, Low voltage applications.

I. INTRODUCTION

The power consumption is the major issue in designing the integrated circuits. Large heat dissipation affects the performance and the reliability. The one more reason for reducing the power dissipation is to increase the battery lifetime. The digital circuits have many D flip-flops. Reduction in power dissipation of it has significant impact on the overall power consumption.

THE rapid growth in deployment of Internet of Things (IoT) devices means that processors are now becoming pervasive. IoT finds applications in various areas including healthcare, smart environments, and transportation. However, along with the widespread deployment of these devices there comes a natural desire to reduce their energy/power demands: this can extend device active times, or mean that their batteries can be made smaller (reducing their cost and size). There is also a need to reduce the cost of device production, and minimizing the silicon area occupied by processors is a key consideration. Scaling down the supply voltage brings power reduction benefits. Sub-threshold techniques adopt aggressive supply voltage scaling, below the threshold voltage, but have a significant impact on variability and performance. In contrast near-threshold voltage (NTV) techniques allow the supply voltage to be brought close to the threshold voltage (but not below it), with a reduced impact on variability and performance characteristics, making this regime of operation more suitable for industry adoption.

Flip-flops (FFs) are essential building blocks of sequential digital circuits but typically occupy a substantial proportion of chip area and consume major power consumption. The basic building blocks of the sequential digital circuit are flip-flops. Another name for flip-flops is bistable circuit, which means it has two stable states ”0” and “1”. When any triggering comes, it makes the circuit to be in one state, and any change of the triggering will cause the flip-flop to change its state, so a trigger pulse must be used into the circuit in order to change the state. Besides that, flipflops use clock signals as control inputs. Each flip-flop stores one bit.

The block diagram of D Flipflop is shown below.

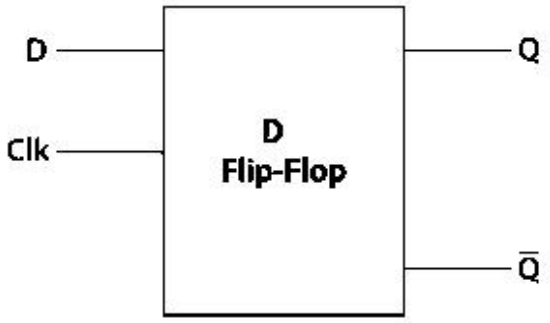

Fig.1 Block diagram of D Flipflop

In D flip flop, the single input "D" is referred to as the "Data" input. When the data input is set to 1, the flip flop would be set, and when it is set to 0, the flip flop would change and become reset. However, this would be pointless since the output of the flip flop would always change on every pulse applied to this data input.

The "CLOCK" input is used to avoid this for isolating the data input from the flip flop's latching circuitry. When the clock input is set to true, the D input condition is only copied to the output Q. This forms the basis of another sequential device referred to as **D Flip Flop**.

When the clock input is set to 1, the "set" and "reset" inputs of the flip-flop are both set to 1. So it will not change the state and store the data present on its output before the clock transition occurred. In simple words, the output is "latched" at either 0 or 1.

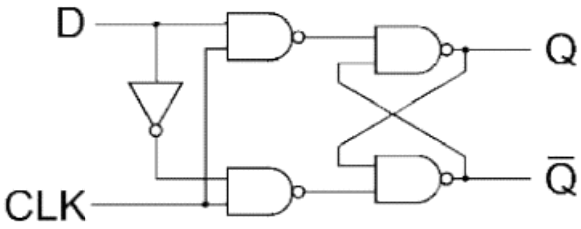

Fig.2 Conventional gate level architecture of D Flipflop

Table:1 Truth table of D flipflop

CLK	D	Q	Qb
0	0	Q	Qb
0	1	Q	Qb
1	0	0	1
1	1	1	0

From the above truth table, it can be observed that when the clk signal is high only, the data present in D input will be transferred to Q output.

Since the performance of Flipflops impacts the application, it is necessary to improve the performance of Flipflop.

II. RELATED WORKS

A static single-phase-clocked contention-free FF (S2CFF) is proposed in this method. Since conventional TSPC FF is based on dynamic logic and the voltage of internal nodes is not retentive, it is not suitable for low voltage operation. In S2CFF, the retentive problem of internal nodes is solved so that the FF can work correctly at low supply voltage. The main drawback of S2CFF is the waste of power consumption in redundant precharge and discharge operations. When the input data D remains 0, the node N2 precharges to VDD throughM7 during the negative half cycle of CK and discharges to GND through M8 and M10 at the rising edge of CK. The precharge and discharge operation does not change the state of the circuit, and the capacitance of the node N2 is quite large, so the operation is redundant and wastes much energy

The circuit diagram of S2CFF is shown below.

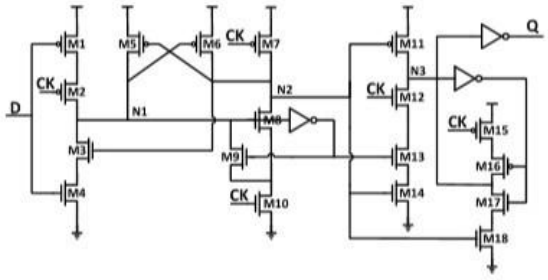

Fig.3 Circuit diagram of S2CFF Flipflop.

As shown in Fig. 3, the precharge operation of the node N2 in S2CFF when the input data remains 0 is unnecessary. To eliminate the energy-wasted operation, the precharge path should be cutoff when D = 0. A PMOS M1 controlled by the inversion of the input data is inserted into the precharge path of the FF as shown in Fig. 4. When the input data is 1, the PMOS M1 is ON and the necessary precharge operation works as usual. When the input data remains 0, the PMOS M1 is OFF and the precharge path is cutoff by the inserted transistor. As a result, the redundant precharge operation is totally removed.

The block diagram of the flipflop by eliminating the precharge scheme is shown below.

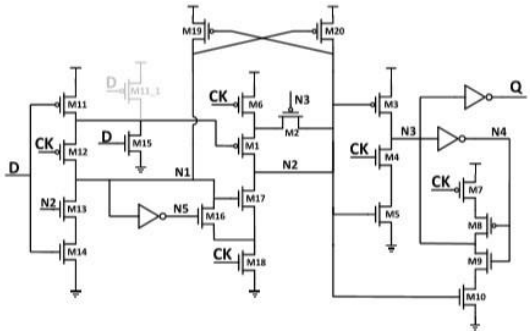

Fig.4. True single phase clock based flipflop

In digital systems, FFs usually need to have additional functions such as set, reset, and scan. These additional functions can be easily added to the proposed FF. The schematic of the proposed FF with such additional functions is shown in Fig. 5

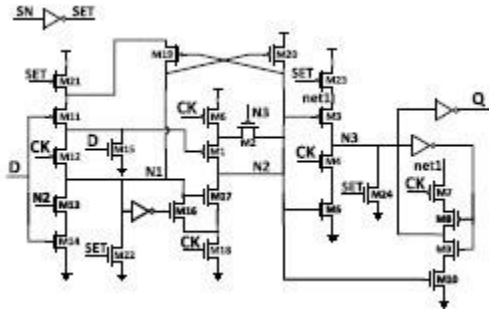

Fig.5: Tspc flipflop with set

As shown in Fig. 5, when the set signal SN is low, SET is high, the charging path of N1 is cutoff by M21, and N1 is pulled down through M22. Since the node N1 is low, N2 is charged to VDD through M20. At the same time, the charging path of N3 is cutoff by M23, N3 is pulled down through M24, and the output keeps high.

Fig.6 shows the schematic of the proposed FF with reset function. As shown in Fig.6, when the reset signal RSTN is low, RST is high, the charging path of N2 is cutoff by M21, and N2 is pulled down through M22. Since N2 is low, N3 is charged to high through M3, and the output Q keeps low. At the same time, N1 is charged to high through M19. A PMOS M23 is inserted to isolate N1 from the input to avoid short circuit current through M12 and M15 when CK=0 and D =1.

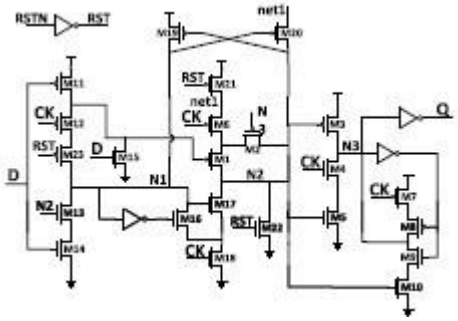

Fig.6 schematic of tspc flipflop with reset.

Fig. 7 shows the schematic of the proposed FF with the scan function. As shown in Fig. 7, when the scan enable signal SE is high, the input data D is isolated from the FF, and the FF captures the data of scan input SI at the rising edge of CK. When SE is low, SI is isolated from the FF, and the FF captures the input data D at the rising edge of CK.

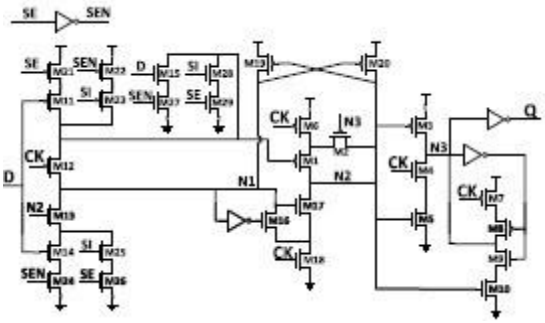

Fig.7 schematic of tspc flipflop with scan input.

As the technology has been scaling down in the recent years, along with the technology, the supply voltage is also being scaled due to which the soft error effect has become the major concern. The schematic of proposed soft error tolerant flip-flop is shown below.

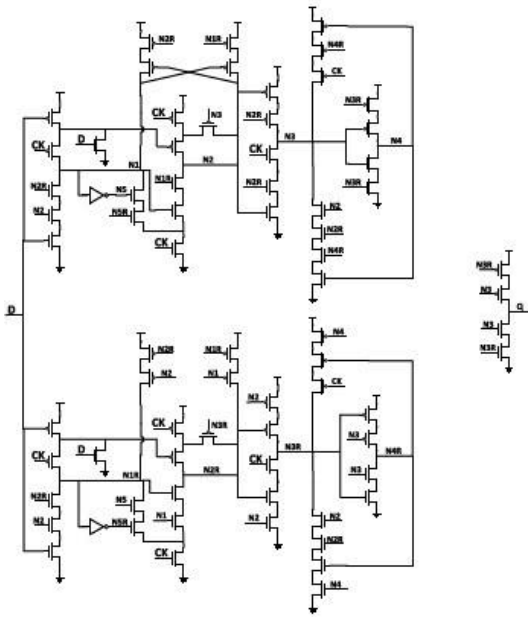

Fig.8: schematic of tspc based soft error tolerant flipflop

III. IMPLEMENTATION

Flipflops are the basic Memory elements in many applications such as registers, counters which are mainly used in portable application. Hence low power consumption is need of the day. Due to technology scaling, the Leakage power consumption is the major concern. To overcome this leakage problem, in this method, header power gating technique is implemented in the proposed TSPC Flipflop. By applying this power gating technique to the flipflop the power consumption is reduced since we are shutting down the power supply when not required.

Sub threshold leakage currents will become an increasingly major component of total power dissipation as future technologies scale and reduce power consumption. One of its most successful leakage power reduction approaches is power gating. In this paper, we offer a power gating technique for Level shifters that allows for power gating during active mode.

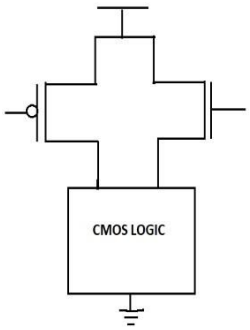

Fig.9: Block diagram of Power Gating

It can be observed from the fig.6 that when the gates of both pmos and nmos are on only the supply will be passed to the circuit.

The circuit diagram of power gated Tspc Flipflop is shown below.

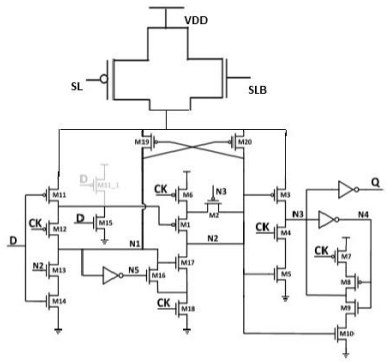

Fig.10: proposed power gated True single phase Flipflop.

IV. CONCLUSION

The design of power gated true single phase clock based flip-flops is presented in this article. Power gating is one of most widely technique for reducing consumption by shutting down the connection from the supply when not required. By applying the power gating concept, power consumption is minimized in the proposed flip-flop design since the supply is passed to the circuit only when required in the proposed d flip-flop design.

V. RESULTS AND DISCUSSIONS

The schematic diagram and waveform of power gated tspc based Flipflop is shown below. Simulations are performed using Tanner EDA tool using 45nm technology.

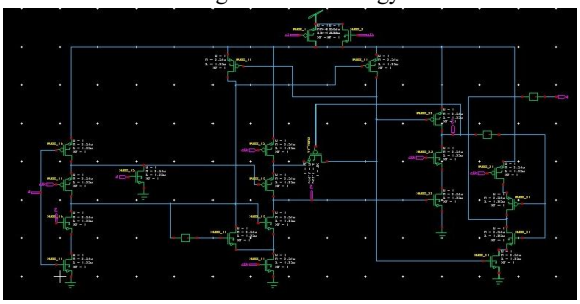

Fig.7 Schematic diagram of Proposed TSPC Flipflop

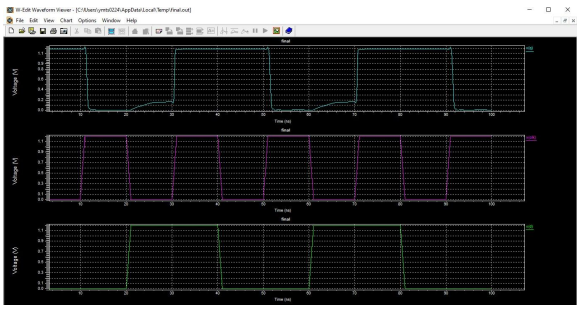

Fig.8: Waveform of proposed SAFF using GDI based latch.

Table 3: Comparison table for Existing and Proposed methods

	Power(uw)	Delay(ns)	Area
Existing flipflop	209	0.7	28
Proposed flipflop	157	0.7	19

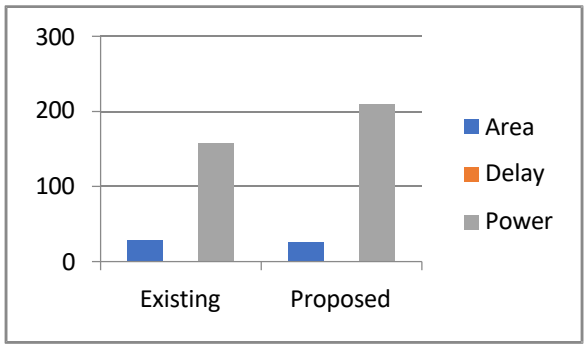

Fig.21 Comparison of area between existing and proposed method

VI. REFERENCES

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