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DESIGN OF LOW POWER HIGH SPEED CMOS D FLIP-FLOP USING HYBRID LOW POWER TECHNIQUES

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ABSTRACT:

The primary goal of this research is to balance low power consumption and high speed performance by designing a low power and high speed CMOS D flip-flop employing hybrid low power approaches. When implementing various types of binary counters, shift registers, and analogue and digital circuit systems, CMOS D flip flops are the preferred choice. Leakage power is the primary significance in CMOS technology. Lowering the supply voltage to the designated circuit in standby mode will lessen power consumption and extend the battery backup time. The CMOS D flip flop circuit uses the SVL approach to suppress signals and lower power dissipation caused by leakage currents in reserve form. Additionally, the suggested design employs fewer clocked transistors, which lowers leakage current and dynamic power consumption to an accessible level. The Cadence Virtuoso tool at 45 nm technology is used to replicate every existing design as well as every proposed design.

Keywords: CMOS, D-Flip Flop, Leakage Power, Le Power Consumption, Power- Delay Product (PDP), Cadence tool.

I. INTRODUCTION

The power consumption is the major issue in designing the integrated circuits. Large power dissipation affects the performance and the reliability. The one more reason for reducing the power dissipation is to increase the battery lifetime. Reduction in power dissipation of it has significant impact on the speed and overall power consumption. Flip-flops are the basic storage elements used in synchronous digital VLSI circuits and in other digital electronic circuits. Bi-stable devices (popularly called Flip-flops) are mostly utilized as solitary bit memory cells.

Flip flop have each of two steady condition, logic 1 or logic 0. We need to trigger the flip flop to get in to any one of two stable states by applying an external pulse as input. The output remains which steady condition until other pulse is utilized to modify to condition. We can also modify the flip flop output by applying proper inputs other than trigger.

Flip flops are widely used in most sequential circuits like counters, shift registers etc…Delay flip flop stores whatever the input bit pattern applied at its D input. This feature helps in processing of data bit by bit by other parts of the digital circuit to get solutions for complex functions. The major drawback of the Set Reset flip flop (i.e. its undeterminable output and if S=R=1) is conquer through the D flip-flop.

D flip-flop, is also known as Data flip-flop since its capability to 'latch' and store data, or Delay flip-flop because latching and accumulate data is utilize to make a impediment in the processing of that data through a circuit. Currently, power consumption of VLSI chips is becoming an increasingly critical problem as modern VLSI circuits continue to grow, and technologies evolve. In portable systems, very low power consumption is desired to increase battery life. Accordingly, for any digital circuit design, power consumption must be taken into account very seriously.

To reduce the complexity of circuit design, a large proportion of digital circuits are synchronous circuits; that is, they operate based on a clock signal. Among the more popular synchronousdigital circuits are D-type flip-flops. The total clock related power consumption in synchronous VLSI circuits can be divided into three major factors: power consumption in the clock network, power consumption in the clock buffers, and power consumption in the D-type flip-flops [5]. It is worth noting that the frequency at which synchronous devices can operate has been limited by clock skew. The greater the frequency of the clock, the smaller the clock skew must be kept maintaining synchronization of the device. It has been observed that clock skew decreases as capacitance on the clock is decreased. Thus, reducing capacitance on the clock line may allow synchronous circuits to operate at higher clock frequencies. Therefore, the improvement of such flip-flops circuits a decreasing in power consumption, without impairing other characteristics, is of prime importance to the VLSI industry. Though several contributions have been made line to the art of DFFs, a need evidently occurs for a design that still further improves the relative power consumption of DFFs.

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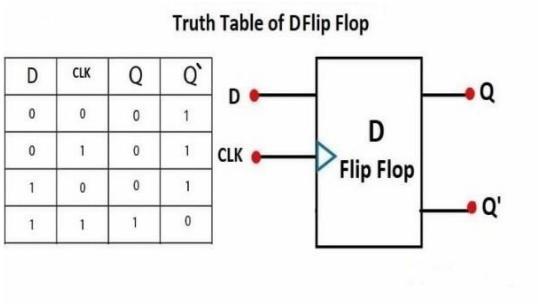
II. IMPLEMENTATION OF DFF

(D FLIP FLOP)



D	CLK	Q	Q`
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Fig 1: Symbol and Truth table of D flip-flop.

1. It consists of two inputs such as data and clock.
2. When clock input is high, the data is transferred to the output of the flip flop and when the clock input is low, the output of the flip flop is held in its previous state.
3. Thus, the output has two stable states based on the inputs which have been discussed below. The D (Data) is the input state for the D flip-flop. The Q and Q' represents output states of the flip-flop.
4. D flip-flops are vital for creating sequential circuits that require the storage and transfer of data in a controlled and synchronized manner.

III. EXISTING METHODS

1. Clock gating &transistor reduction method

The existing clock gating &transistor reduction method is the method which is to discuss as first method. Here in this method the time delay and power issues are discussed with the following schematic circuit of existing Conventional D flip flop as follows:

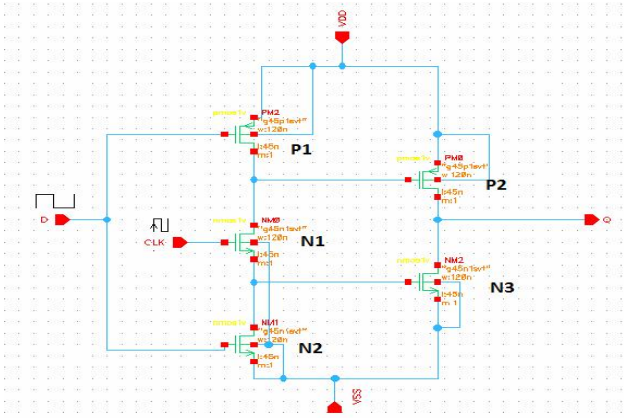


Fig 2: Schematic of conventional D flip-flop.

The results of the Conventional D flip flop is shown in the following figure.

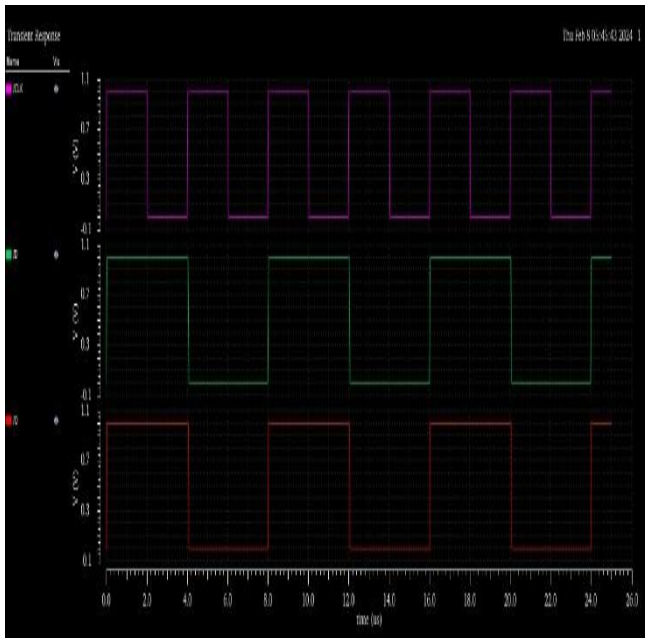


Fig 3: Simulation results of conventional D flip-flop.

Here, we observe that the wave forms are generated for the Conventional D flip flop. The total design of this method is made over by using cadence tool. The time delay and power of the circuit will be discussed at the result section.

2. Self-Voltage Level (SVL) technique

SVL is the acronym for Self Voltage Level. SVL technique is used to reduce leakage power in clocked systems like flip flops during standby mode of operation i.e when clock=0.SVL technique uses a PMOS and a NMOS transistor in parallel as pull up network as well as pull down network as shown in the Fig. 4. Pull up transistors gate is connected with complement of clock signal and pull down transistors gate terminal is connected with clock .This technique to reduce leakage power uses a clock signal as the control signal to control supply voltage to D flip flop. Hence the name self-voltage level is justified. This flip flop uses minimum number of clocked transistors and overcomes the drawbacks of dynamic logic family with improved delay and power delay product parameters. The following figure shows the schematic of D flip fllop with svl technique which includes the invertor gates and transistors to design the D flip flop schematic circuit that describes the previous means the existing method of D flip flop.

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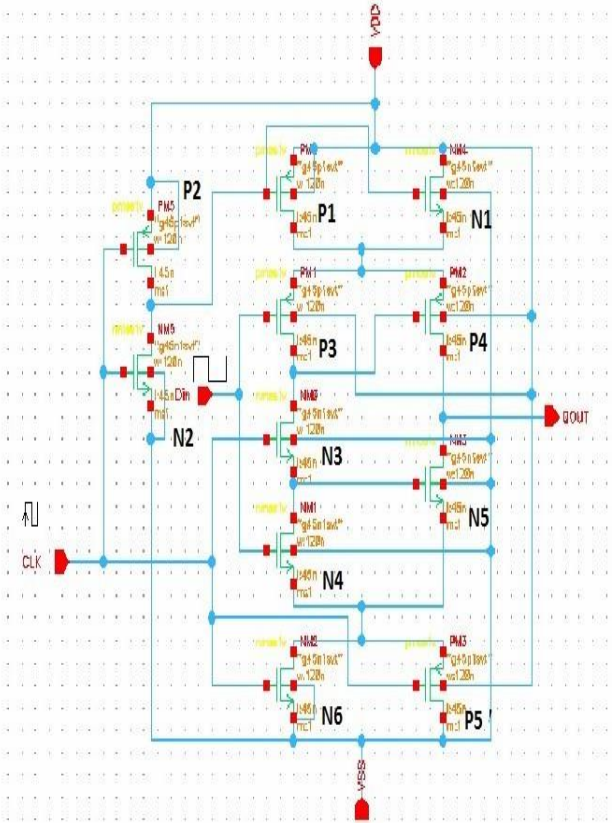

Fig 4: Schematic of D flip flop with SVL technique.

The results of the D flip flop with SVL technique are shown in the following figure.

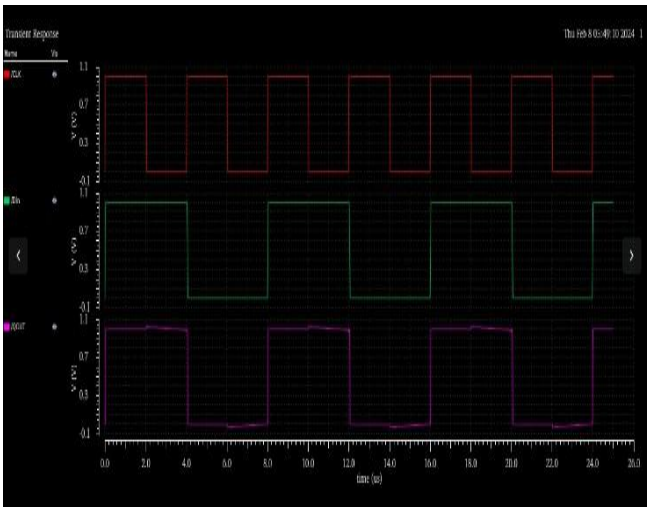

Fig 5: Simulation results of D flip flop with SVL technique.

The following Fig. 4 shows the D flip flop design using SVL technique. The D flip flop is implemented using five transistors, two PMOS (P1 and P2) and three NMOS transistors (N1, N2 and N3)

Case1: Clock = 1(active mode)

Psw1 is ON, Nsw2 is ON , Psw2 is OFF ,Nsw1 is OFF. D flip flop is connected to Vdd and ground for normal circuit operation. If Din=0, P1, N1, N3 are ON and P2, N2 are OFF, connecting Q to ground i.e Q = 0 If Din=1, P1, N3 are in OFF state and N1, N2, P2 are in ON state , connecting Q to Vdd i.e Q = 1

Case2: clock = 0(standby mode)

Psw1, Nsw3 are in OFF state i.e open circuits. Nsw1, Nsw2 are ON but as they are used as pull up they provide Vdd- Vth as the supply voltage for D flip flop. Due to stack of two NMOS transistors sub threshold leakage current is reduced.

Similarly Psw2, Psw3 are ON but as they are used as pull down they provide finite positive voltage instead of ground (0volts).This virtual ground positive voltage slightly reverse biases the NMOS transistors of D flip flop and reduces leakage power [5] in standby mode. For PMOS transistors of D flipflop leakage power is reduced, since they are connected to virtual supply in standby mode.

The results of DFF with SVL technique circuit are given as follows:

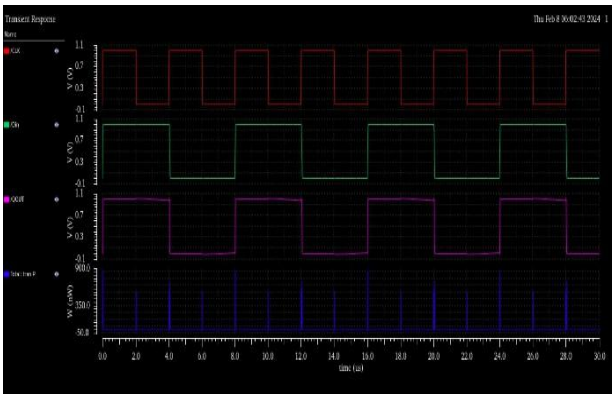

Fig 6: Simulation results of DFF with SVL technique.

In this we can observe the waveforms of the circuit. In T-Spice we can know power consumption and delay values.The time delay and power of the circuit will be discussed in the results section.

3. Improved SVL Technique

The Improved SVL approach, which employs stacked transistors, decreases supply voltage while also lowering leakage current flow. The Improved SVL approach reduces leakage power in standby mode because leakage power consumption in static mode is inversely related to supply voltage and supply current. Schematic of D flip flop with Improved SVL technique is shown in the followingfigure.

For designing the circuits we used Cadence Virtuoso tool. In Cadence we have S-Edit, W-Edit and T-Spice tools. S- Edit means schematic editor, where we can draw the schematic diagram of the circuit. W-Edit means waveform editor. In this we can observe the waveforms of the circuit. In T-Spice we can know power consumption and delay values. Output waveforms of D flip flop using ASVL technique are shown in Fig.7. The power consumed, delay and PDP (product of delay and power) are shown in table.

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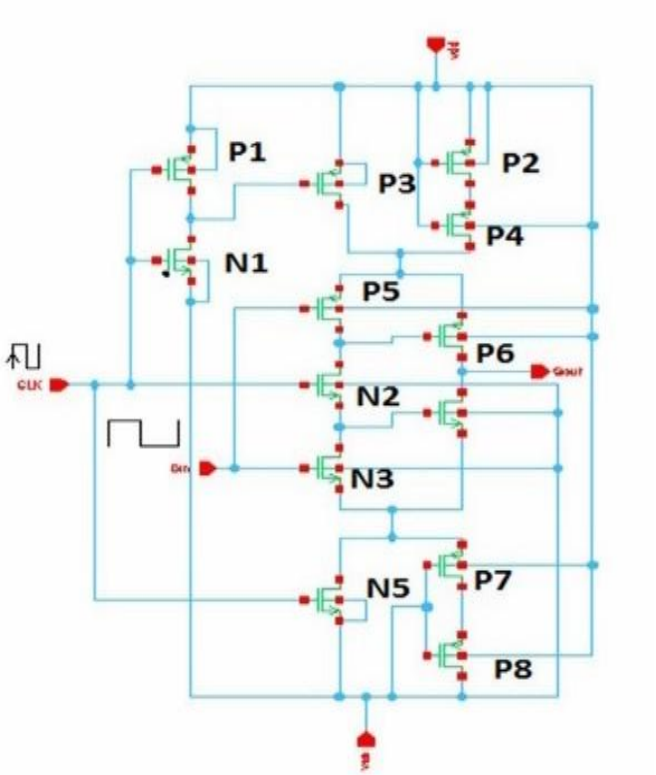

ue.

The following Fig. 4 shows the D flip flop design using Improved Self Voltage Level (ISVL) technique.

The Figure 3 visualizes the Delay FlipFlop structure utilizing enhanced SVL method. The DFPFP is designed utilizing five transistors; those are two PMOS transistors (P1 & P2) and three NMOS transistors (N1, N2 &N3). This also contains two cases, the first case is if the clock given is '1' which is in active mode such that P1 gets ON, N2 gets ON, and P2,P3 gets OFF and N1, N2 gets OFF. Then DFPFP gets joints to Vdd and ground for normal circuit operation. And while Din is zero Pl, N1, N3 gets on and P2, N2 gets off, such that 'Q' connects to ground then a becomes Zero. And if Din is '1' ON then P1, N3 gets off and N1, N2 and P2 gets ON such that output Q joints to Vdd then Q becomes '1'.

The second case is such that is clock given is '1' which operates in standby mode, so that P1, N3 gets off operates open switch. NI, N2 gets ON because of transistors in pull up it shows VDD - Vth as supply potential to Flipflop (DFPFP). At the time of extra two NMOS transistors internally related to threshold current gets shortened.

In the same way P2, P3 gets ON which are in pull down gets limited positive Potential rather than ground which is at zero volts. If the virtual ground positive potential is moderately reverse bias to NMOS transistors of DFPFP, such that optimizes power dissipation because of DFPFP, such that optimizes power dissipation because of DFPFP is in standby mode. The PMOS transistors of DFPFP leakage power gets optimized, because those are jointed to virtual supply which is in standby mode.

In SVL method, the power dissipation gets optimized in addition leakage current flow also gets minimized because of the connection of extra two transistors. The basic is that supply potential for the flip-flop design is substantially optimized in static mode.

The flip-flop design is substantially optimized in static mode. The power dissipation at ideal condition is directly connected to supply potential and current, such that power dissipation is shortened for same value because of enhanced SVL method. Because of projected SVL technique the power dissipation gets optimized, in addition count of clocked transistors gets minimized. Hence working speed of design increases and also the dynamic power consumption gets optimized. So this method of DFPFP in standby mode is utilized to reduce power consumption.

Since leakage power consumption in static mode is directly proportional to the supply voltage and supply current, thus leakage power is reduced in standby mode using Improved SVL Technique.

In addition to leakage power reduction in our design we also reduced no. of clocked transistors which helps in speeding up the operation of the circuit and also contributes a little in reducing dynamic power consumption also. Though we have used this technique for D Flip Flop it's obvious that we can use technique for any clocked circuit to reduce leakage power in static mode.

The Figure 7 and 8 visualizes the schematic diagram and simulated outcomes of utilizing Improved SVL technique.

The results of the D flip flop with Improved SVL technique are shown in the following figure.

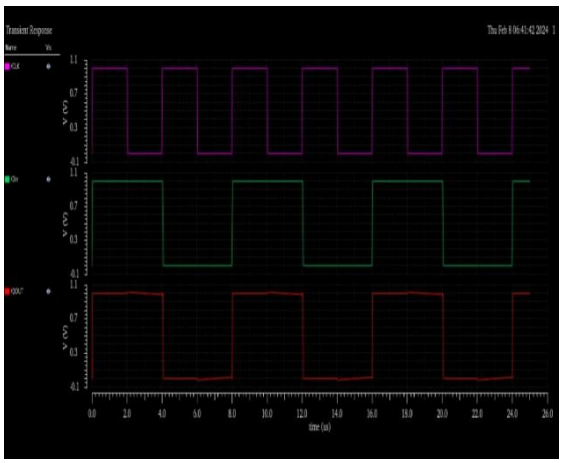

Fig. 8 Simulation results of D flip flop with Improved SVL technique.

IV. PROPOSED METHODS

Modified SVL Technique

The modified SVL approach, which employs stacked transistors, decreases supply voltage while also lowering leakage current flow. The Altered SVL approach reduces leakage power in standby mode because leakage power consumption in static mode is inversely related to supply voltage and supply current. Two instances are shown in this altered SVL technique.

In our proposed work in addition to reducing leakage power, we also decreased the number of transistors, which speeds up circuit operation and also lowers the static and dynamic power consumption.

Case 1: Clk=1(active mode)

Because Psw1 and Nsw2 are coupled in a pull-up session, the supply voltage drop is Vdd-Vth, and Psw2 is switched on. If D in = 0 and Clk = 1, P1 and N3 are ON, while P2 and N2 are OFF. If N3 is turned on, we can argue that Q connects to ground or that Q=0. If D in=1 and Clk=1, then P1,N3 are off, N1,N2 and P2 are on, and Q connects to the supply (Q=1)

.

Case 2: Clk=0(Standby mode)

Psw1, Nsw2 are in OFF condition and Nsw1 is ON, as it is Connected to Supply and it is in pull-up session, it provides Vdd-Vth Supply voltage. Psw2 is Connected to g ground and it contains the positive voltage.

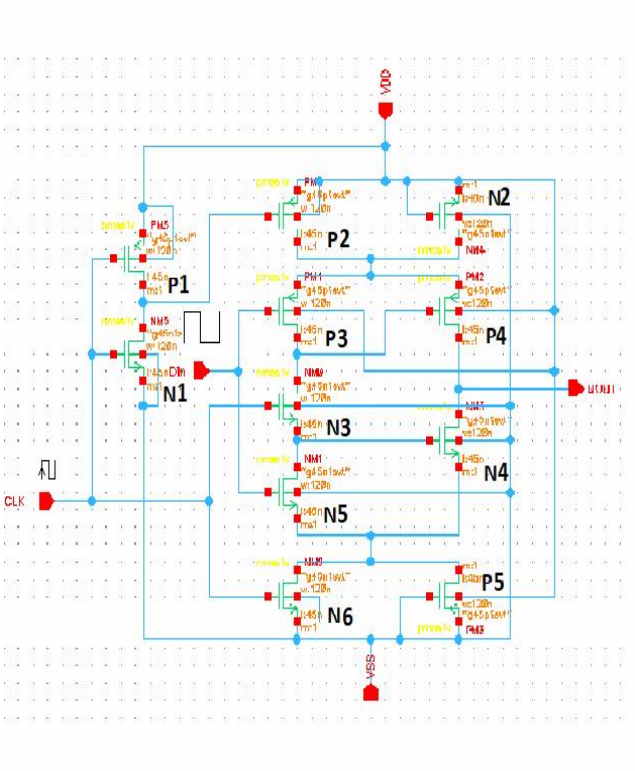

Fig 9: Schematic of D flip flop with ASVL technique.

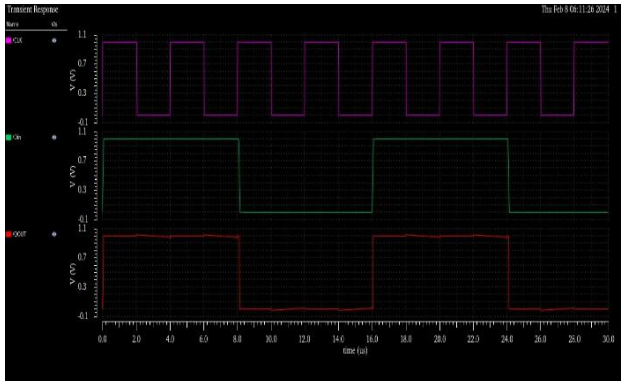

Fig 10: Simulation results of D flip flop with MSVL technique.

Here, we observe that the above figures describes the analog simulation implementation and power graph of DFF using Cadence. The last waveform in the above simulated result illustrates the power consumed for the above circuit. In addition to leakage power reduction in our proposed design we also reduced no. of Clocked transistors which helps in speeding up the operation of the circuit and also contributes a little in reducing dynamic power consumption also. Though we have used this technique for D Flip Flop it's obvious that we can use technique for any clocked circuit to reduce leakage power in static mode.

The power graph for proposed method is shown below:

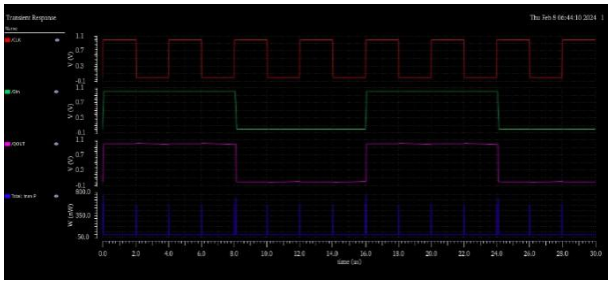

Fig 11: Power graph of proposed DFF.

V. RESULTS AND DISCUSSION

Table I: Comparison of Results:

Name of the Flip-flop	Average Power(μW)	Time Delay(ns)
Conventional D flip flop	904.81	524
DFF with SVL	863.57	470
DFF with ISVL	832.29	392
DFF with MSVL	752.68	296

From the comparison table, we observe that difference between the existing method flip flops and newly proposed flip flop in terms of power and time delay. The first method, Conventional D flip flop has consumed high power 904.81(nW) compared to the other flip flops. The second method is DFF with SVL which consumes 863.57(nW) power, here when compared to the first one the power consumption is low. The third one DFF with ASVL which consumes 832.29 (nW) power which is lower than above two methods. Finally, the newly proposed method which consumes low power 752.68(nW) compared to all the existing methods and at the same time, the number of transistors is also minimized in this method. So, the newly proposed method will run at low power with high speed which can be used for low power digitalsystem applications.

VII. CONCLUSION

The consumption of power in the D flip-flop is minimized by using the proposed method. In conclusion, the newly designed D flip flop can be effectively used low power digital system applications for storage purpose. It has been observed that a significant amount of power consumption is generated by the clock line. This paper compares four previously published DFFs together with our design for different metrics. As compared to three previously published DFFs, our design outperforms in terms of power consumption and power-delay-product. Especially, the proposed flip-flop is superior in power reduction at different parameters, hence, it is well suited for low-power digital system applications.

VIII. REFERENCES

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