DSP Program Based Controller for 9 Level Inverter Topology

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ABSTRACT

This paper presents an improved sensor less nine-level inverter topology with reduced number of components. It is formed by cascading a three-level T-type neutral clamped point inverter with a floating capacitor (FC) fed two-level converter unit. Additionally, two line-frequency switches are appended across the dc-link. A simple DSP program based controller is designed which is in-charge of maintaining the FC voltage at its reference value without any aid of voltage and current sensor. Thus, the complexity in control of the proposed topology is very minimal. The working principle of the proposed inverter is deliberated in detail. Furthermore, the simulation results presented to validate feasibility and operability of the proposed topology. Finally, a comprehensive comparison with recently reported inverter topologies proving the merits of the proposed topology is included.

Keywords: Multilevel inverter (MLI), power quality, self voltage balancing, switched capacitor (SC) etc.

1. INTRODUCTION

Multilevel inverters (MLIs) have been extensively investigated during the recent past and are undoubtedly the emerging solution for a variety of power electronics applications owing to their propitious features like improved power quality, reduced device stress, high modularity, reduced filter requirement, etc., [1]. The traditional MLIs predominantly used are cascaded H-bridge, neutral-point-clamped (NPC), modular MLI, flying capacitor inverters, and their variants [2]. However, recently the use of MLIs as power interface for low power applications like grid connected renewable energy sources has become more prevalent [3]–[5]. Following the commercial availability of power devices (MOSFETs and insulated gate bipolar transistor (IGBTs)) with a voltage rating up to 1.2 kV sufficing the low-power applications, a rapid research on new MLI topologies with a pertinent focus on reducing the number of part count (switches, capacitors, and diodes) is witnessed [6].

Use of switched dc sources for the generation of a multistep waveform is the pre-eminent idea of multilevel dc–ac power conversion [7]. In the recent past, attempts have been made to separate the level and polarity generation part to reduce the number of dc sources and power switches for a given number of voltage levels [8], [9]. On the other hand, many hybrid topologies combining the traditional and not-so-traditional MLIs are found in the literature. A floating capacitor (FC) based single dc source multicell converter capable of doubling the rms output voltage is presented in [10]. In [11], cascade connection of a five-level (5L) double flying capacitor multicell converter and a floating capacitor (FC) fed H-bridge resulting in a nine-level (9L) output voltage is proposed. It requires single dc source, ten switches, and two capacitors for its operation.

A single dc source switched capacitor (SC) based MLI proposed in [12] comprises two capacitors, nine switches, and two diodes. An use of MLI for transformerless grid-connected photovoltaic (PV) system is demonstrated in [13]. Furthermore, many topologies advocating the usage of T-type NPC (TNPC) MLI as an integral part of the overall inverter structure is found widespread [14]. A TNPC MLI in cascade with an

FC Hbridge topology proposed in [15] requires ten switches, and one FC is proclaimed to have the least number of switches and capacitors.

This letter adds-on to the research carried out in [15] by offering a further reduction in the number of switches thereby demonstrates a decline in the number of on-state switches and gate drivers. A sensorless voltage balancing strategy embedded within the switching control is developed to regulate the voltage across FC around its reference value. Simple logic-form equations-based switching functions are formulated for the generation of gating signals and thus are faster than cost function optimization methods. The experimental results obtained from the developed laboratory prototype are presented to validate the theoretical concepts. Finally, a comparative study against a few of recently reported potential topologies is carried out to highlight the advantages of the proposed topology. The circuit configuration of the proposed hybrid 9L reduced part count inverter is shown in Fig. 1. It includes the following power electronic building blocks.

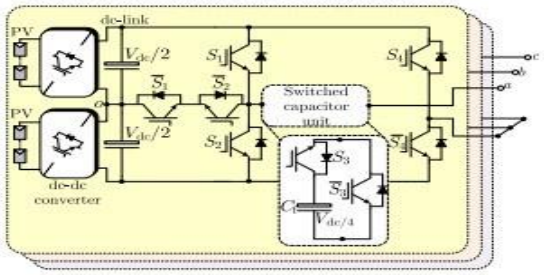

Figure 1. Power circuit schematic of the proposed 9L topology

1) *TNPC inverter*: It serves as a fundamental multilevel voltage generation unit capable of producing three unique voltage levels namely Vdc/2, 0, −Vdc/2. The switches S1 , S2 , $S^{-}1$, and $S^{-}2$ constitute the TNPC unit, which are required to block a voltage of Vdc for S1 , S2 , and Vdc/2 for $S^{-}1$ and $S^{-}2$, respectively.

2) *SC unit:* It is basically a two-level (2L) voltage converter capable of generating levels 0 and Vdc/4, comprising the switches S3 , $S^{-}3$, and an FC Cf , whose voltage (vC) need to be regulated at one-fourth of the total dc-link voltage, i.e., Vdc/4 for the generation of output voltage with uniform steps.

3) *Line frequency switches (LFSs):* Two switches (S4 and $S^{-}4$) operating at line frequency is connected across the dc-link. The principal function of this unit is to add Vdc to the 5L voltage generated by the series connected TNPC and SC unit. Consequently, a 9L voltage waveform is synthesized. In other words, the addition of LFSs doubles the number of voltage levels generated by the latter combination. In an ideal circumstance, the proposed inverter can generate 9L output voltage: ±Vdc, ±3Vdc/4, ±Vdc/2, ±Vdc/4, and 0, requiring only eight switches and one FC, which is the least number of components required for an SC-based 9L topologies reported till date. In the proposed inverter, the number of on-state switches ranges from three to four, while one of them operating at line frequency supplements the fact of an improved efficiency. Nonetheless, this reduction in number power switches has a disparate effect on the number of overall redundant switching states as evident from Table I. However, a keen observation of Table I reveals the fact that charging and discharging time interval of the FC are identical over a cycle of output voltage.

Table (1) Switching States and Their Effect On Fc Voltage At Each Output Voltage Level

Voltage levels	S_1	S_2	S_3	S_4	FC voltage
V_{dc}	1	0	0	0	No effect
$3V_{dc}/4$	1	0	1	0	Charging
$V_{dc}/2$	0	0	0	0	No effect
$V_{dc}/4$	0	0	1	0	Charging
0	0/1	1/0	0	0/1	No effect
$-V_{dc}/4$	1	0	1	1	Discharging
$-V_{dc}/2$	0	0	0	1	No effect
$-3V_{dc}/4$	0	0	1	1	Discharging
$-V_{dc}$	0	1	0	1	No effect

2. EXISTING SYSTEM

A. Logic-Form Equations-Based FC Voltage Control In this letter, the fundamental frequency switching is used for generating the gate pulses. The selection of this particular method is to validate the operation of the proposed inverter and to describe the rationale behind the formulation of the logical expressions in a straightforward way. The transition angles are obtained using

$$\theta_n = \sin^{-1}\left(\frac{2n-1}{N_l}\right), n = 1, 2, \ldots, \frac{N_l - 1}{2}, 0 \le \theta_n \le \frac{\pi}{2}$$

where Nl is the number of output voltage levels. Nevertheless, other methods like selective harmonic elimination or selective harmonic minimization can be used to compute these angles. The peak value of the reference voltage vref = vm sin(ωt) is generated by the controller as per the control input. The multilevel output voltage derived by comparing the reference voltage with the dc offsets is depicted in Fig. 2;

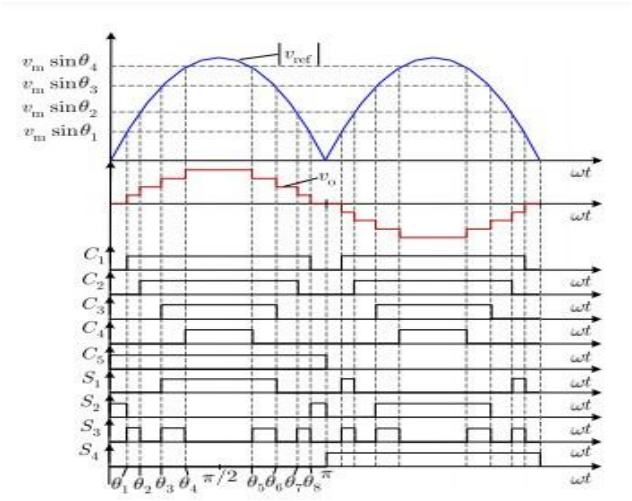

Figure 2. Reference voltage, output voltage, and gate pulses of the existing MLI operated using fundamental switching method.

where C1 − C5 corresponds to the comparison outputs of the five comparators. comparator outputs and are expressed as

$$SF\ 1 = (C3 \times C5) + (C1 \times \bar{C}2 \times \bar{C}5)$$

$$SF\ 2 = (C1 \times \bar{C}2 \times C5) + (C3 \times \bar{C}5)$$

$$SF\ 3 = (C1 \times \bar{C}2) + (C3 \times \bar{C}4)$$

$$SF\ 4 = \bar{C}5 \quad (5)$$

where operator "×" and "+" corresponds to logical AND and logical OR operations, respectively. It is worth mentioning that the developed controller embedding the logic-form equations is adaptable for other well established PWM techniques and does not involve cost function minimization.

3. PROPOSED METHOD

Using switching combinations enlisted in Table I, A simple DSP programming controller is designed which is in-charge of maintaining the FC voltage at its reference value without any aid of voltage and current sensor. Thus, the complexity in control of the proposed topology is very minimal. The corresponding gating signals are so derived from matching the output voltage depicted in Fig. 3 with DSP programing on the Fig. 3. Reference voltage, output voltage, and gate pulses of the proposed MLI operated using fundamental switching method.

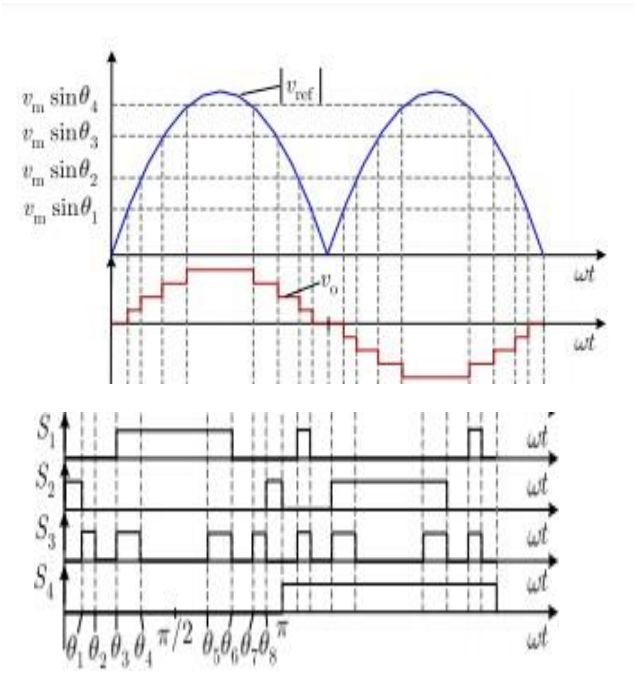

Figure 3. Reference voltage, output voltage, and gate pulses of the proposed MLI operated using fundamental switching method.

4. SIMULATION RESULTS

A. Existing System

The simulation for analyzing the results is obtained from MATLAB software. The simulation diagram of a Existing Method is shown in the figure below 4. The figure 5 to figure 9 shows the corresponding simulink model of voltages and currents show in below.

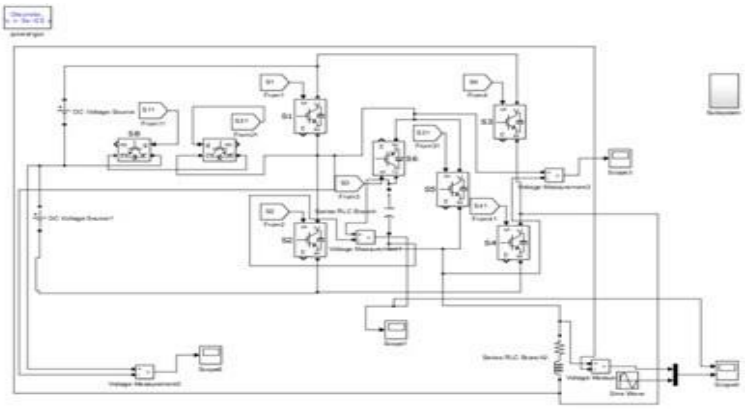

Figure 4. Simulink Diagram

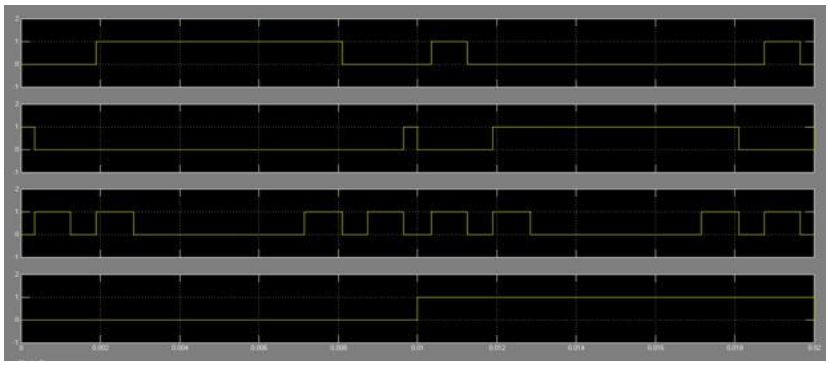

Figure 5. Gate Pulses

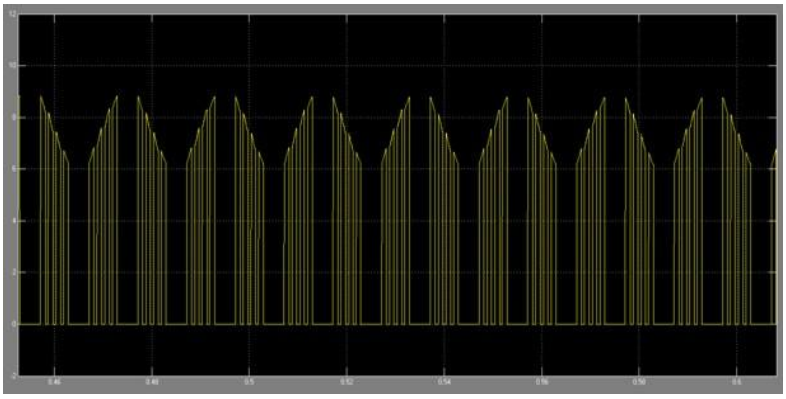

Figure 6. Voltage across SCU

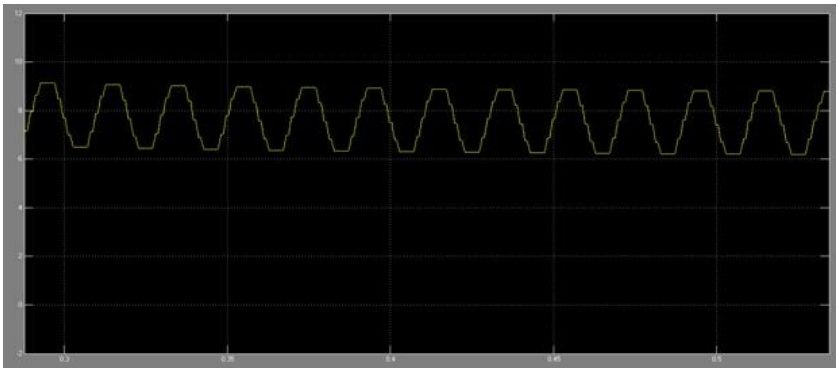

Figure 7. Voltage across FC

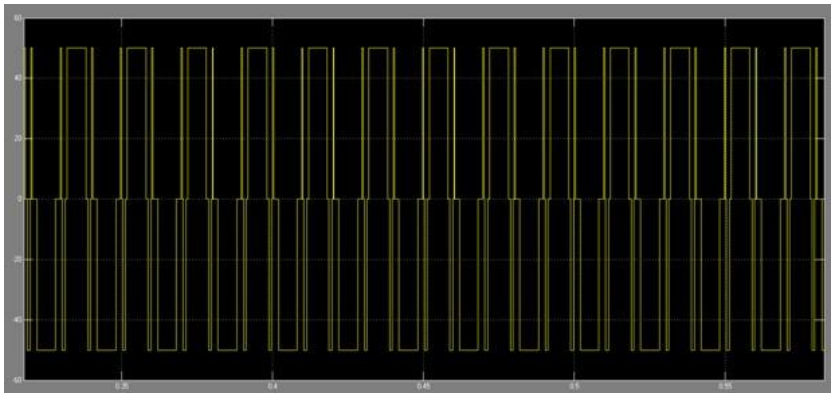

Figure 8. Voltage across TNPC

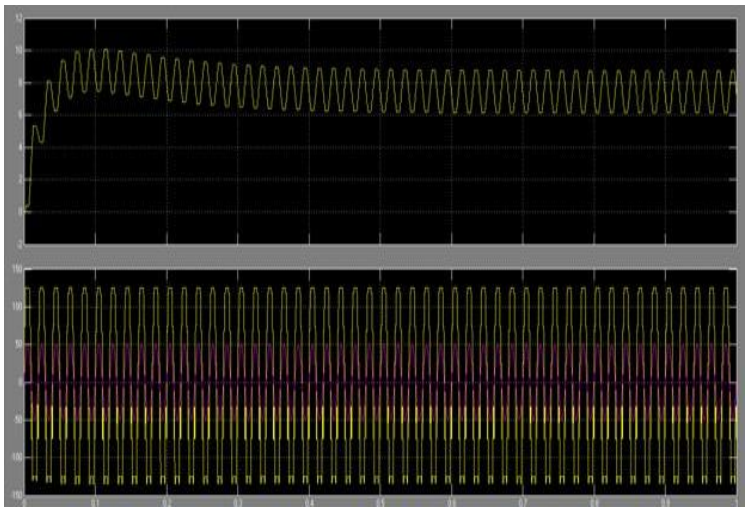

Figure 9. Voltage across FC and Load Currents

B. Proposed System

The simulation for analyzing the results is obtained from MATLAB software. The simulation diagram of a Proposed Method is shown in the figure below 10. The figure 11 to figure 14 shows the corresponding simulink model of voltages and currents show in below.

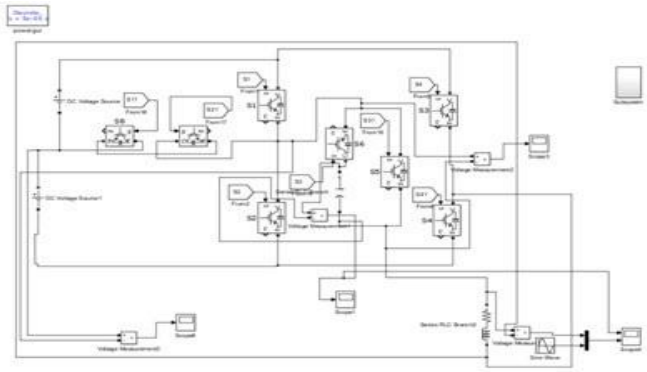

Figure 10. Simulation diagram

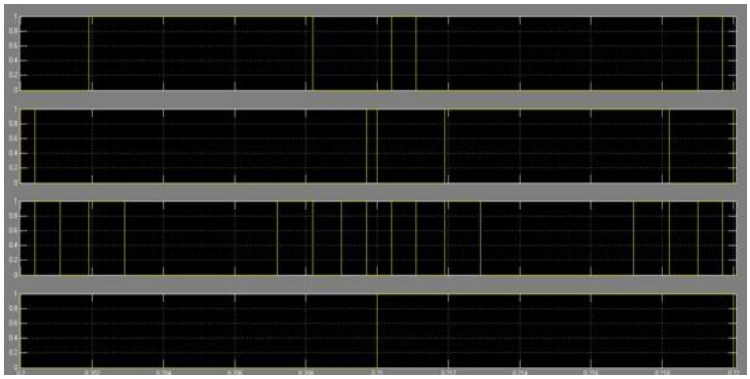

Figure 11. Gate pulses

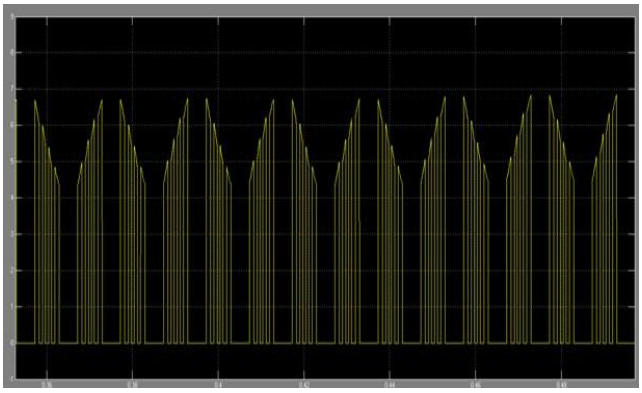

Figure 12. Voltage across SCU

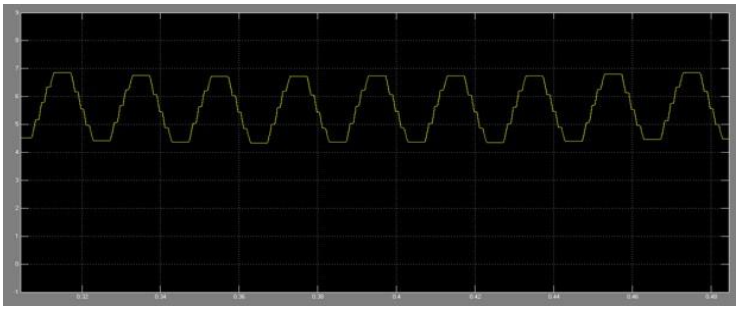

Figure 13. Voltage across FC

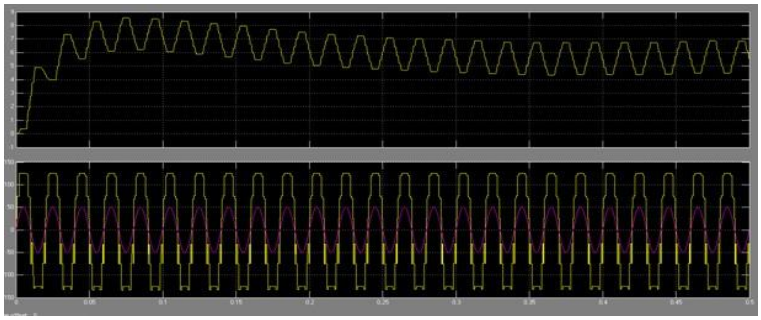

Figure 14. Voltage across FC and Load Currents

Table (2): Comparison Between Existing and Proposed Systems

S.NO	Parameter	Existing System	Proposed System
1	No of switches	8	8
2	Switching technique	Logic form equations	DSP program based controller
3	Voltage ripple	High	Low
4	Switching stress	High	Low
5	Complexity	More	Simple
6	Efficiency	83.5	84

5. CONCLUSION

In this paper, the working concept of the proposed 9L SC based MLI was discussed and verified with matlab simulink. The topology is highly compact comprising of eight switches (while two of them operate at line frequency) and one FC. Also, the number of current conducting switches are less in comparison to other 9L topologies. Due to the inherent self-balancing capability, the voltage across FC ideally remains constant at all operating conditions. Besides, the developed dsp programing based controller does not involve any cost function minimization or complex computations and thus simplifies its real-time implementation. A wide-ranging comparison regarding total blocking voltage and price factors verifies the

superior performance of the proposed inverter with recently acclaimed topologies. The capability to generate a multilevel output voltage and lower power electronics cost requirement enables the presented topology to be a challenging candidate for the conventional grid-connected inverters.

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