International Journal of Research in Science advanced Technology and management studies (IJRSTMS)

ISSN: 2459-425X • Website: www.ijrstms.com

PARALLEL OPERATION OF DOUBLE STEPDOWN DC-DC CONVERTER

Dr.CHEN CHOU, Dr.BUCIO PITTY,

PG Scholar, Sathyabhama University[1] ,Chennai

PG Scholar, Sathyabhama University[2] ,Chennai

ABSTRACT

In this project, double step-down DC-DC converter with high efficiency and high step-down function is proposed. The proposed converter has a double step-down feature with reduced voltage stress at the primary side of the transformer .Without adding complexity to the hardware and control, the proposed converter inherently prevents transformer saturation problem caused by the DC component of the transformer. Moreover, voltage stress of three primary side switches reduces to half of the input voltage and zero voltage switching (ZVS) is naturally achieved for all switches with lower output capacitor energy of the switches. An experimental prototype is developed

***Index Terms*—Double step-down, full-bridge converter, phase-shift, transformer saturation, zero voltage switching**

I. INTRODUCTION

DC-DC converters are electronic devices used whenever we want to change DC electrical power efficiently from one voltage level to another. They are needed because unlike AC, DC cannot simply be stepped up or down using a transformer. In many ways, a DC-DC converter is the DC equivalent of a transformer .In many of these applications, we want to change the DC energy from one voltage level to another, while wasting as little as possible in the process. In other words, we want to perform the conversion with the highest possible efficiency. An important point to remember about all DC-DC converters is that like a transformer, they essentially just change the input energy into a different impedance level. So whatever the output voltage level, the output power all comes from the input; there is no energy manufactured inside the converter. Quite the contrary, in fact some is inevitably used up by the converter circuitry and components, in doing their job. We can therefore represent the basic power flow in a converter with this equation Pin = Pout + P (losses) .Of course if we had a perfect converter, it would behave in the same way as a perfect transformer. There would be no losses, and Pout would be exactly the same as Pin.

We could then say that: V in x I in = V out x I out. However, the double step-down converters in were only applied to non-isolated DCDC converter and has not been explored in the transformer isolated DC-DC converter. In this paper, an isolated double step-down DC-DC converter is proposed. The proposed converter features wider ZVS range and does not have transformer saturation problem. To verify the performances of the proposed converter, a 3 kW prototype has been built and tested.

DOUBLE STEP DOWN CONVERTER

The double step down is applied for non–isolated dc-dc converter and formerly not used in transformers. Here there is no transformer saturation problem since implemented parallel. Due to parallel operation if one gets failed the other works and There is continuity in operation. DC blocking capacitor is generally connected in series with the transformer to avoid transformer saturation problem. Addition of one extra capacitor the converter has following advantages over the conventional two-phase interleaved DC- DC converter. First, there is no current unbalance problem between $L1$ and $L2$ due to the charge (amp-sec) balance condition of the Ci. Therefore, no additional current sensing circuit and control scheme is required. Secondly, voltage stress of the three switches becomes half of input voltage.

BOOST MODE OF OPERATION

International Journal of Research in Science advanced Technology and management studies (IJRSTMS)

ISSN: 2459-425X • Website: www.ijrstms.com

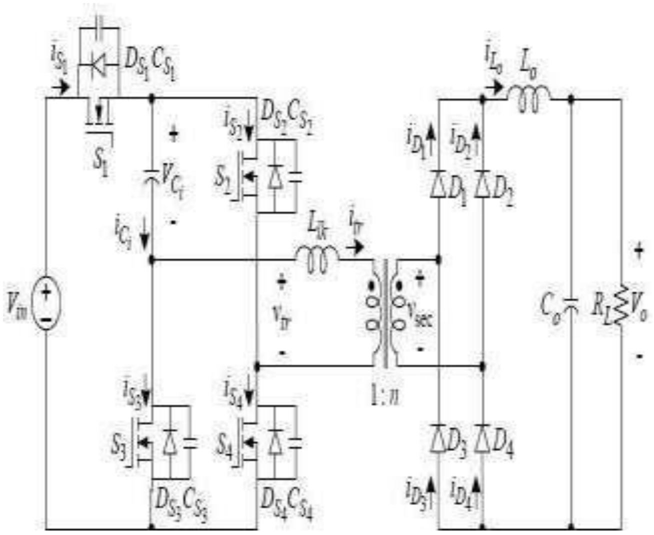

Fig.1.Double stepdown converter

Fig.2 shows the boost converter. In boost mode, output voltage is stepped up. During this mode switch S1 & diode D2 turned ON. The energy is transferred from low voltage.The current rises in the inductor due to V and the energy is stored in the inductor. When the switch S2 & D1 are turned ON. The inductor discharge and its energy is added with the input voltage VL. This increased voltage is applied to the motor. The energy is transferred in forward direction.

A boost converter (step-up converter) is a DC-to-DC power converter that steps up voltage (while stepping down current) from its input (supply) to its output (load). It is a class of switched-mode power supply (SMPS) containing at least two semiconductors (a diode and a transistor) and at least one energy storage element: a capacitor, inductor, or the two in combination. To reduce voltage ripple, filters made of capacitors (sometimes in combination with inductors) are normally added to such a converter's output (load-side filter) and input (supplyside filter).

2 The below figure shows the Boost converter with switches S1; S2 with Resistive load at the end.

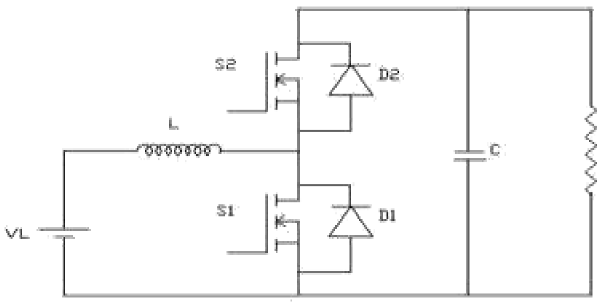

Fig.2 Boost converter

International Journal of Research in Science advanced Technology and management studies (IJRSTMS)

ISSN: 2459-425X • Website: www.ijrstms.com

BUCK MODE OF OPERATION

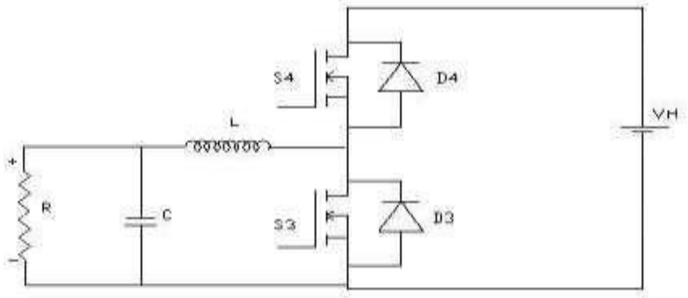

Fig.3 Buck converter

Fig.3 shows the buck converter. The switches S3 and S4 are controlled instantly by means of pulse width modulation technique simultaneously by varying the duty cycle. During the buck operating mode, switch S4 and diode D3 is turned ON. Now energy is transferred from VH to VL .The energy is transferred in reverse direction.

ZVS CHARACTERISTICS

In the conventional PS-PWM converter, all the switch voltages are changing from *V in* to zero. However, in the proposed converter switch voltages are changing from *VIN* /2 to zero. Although the voltage stress of the switch *S*2 is equal to, its voltage transition at the instant of switching is also from *VIN* /2 to zero or from *VIN* to *VIN* / 2. Therefore, all the switch voltage transition in the proposed converter is reduced to half of the conventional PS-PWM converter and this unique feature contributes to the extension of ZVS range in the proposed converter. It is well known that most of the soft switching PWM converters use *L* for soft switching and extra inductor is sometimes used if *L* is not sufficient. Thus, from transformer (or load) current required for ZVS is also reduced to half if we assume the same *C* in both cases .As depicted in Figure in the conventional PS-PWM converter, the two phase arms have different ZVS condition. The phase leg comprising S1 and *S*3 has lower transformer current at the instant of switching than the phase leg comprising *S*2 and *S*4 .Therefore, the ZVS range of converter is determined by the phase leg comprising *S*1 and *S*3 .However, in the proposed converter as depicted in Figure, the switches *S*3 and *S*4 have higher transformer current than *S*1 and *S*2 at the instant of switching.

AUTOMATIC REMOVAL OF TRANSFORMER SATURATION PROBLEM

It is well known that conventional bridge-type converters have transformer saturation problem due to the slightly different time delays in gate drive circuitry or in switching devices. However, the proposed converter can solve this problem automatically for the following reason. In addition, the *Ci* current constitutes part of the transformer current. To avoid transformer saturation, the two areas (area 1 and 2) in must be the same. In the proposed converter, with the addition of *Ci*, the two areas becomes the same due to the charge (amp-sec) balance condition

3

on the *Ci.* As a result, the saturation of transformer is removed automatically and completely. Due to absence of transformer saturation problem the efficiency of the proposed network is also good.

International Journal of Research in Science advanced Technology and management studies (IJRSTMS)

ISSN: 2459-425X • Website: www.ijrstms.com

II. SIMULATION RESULTS

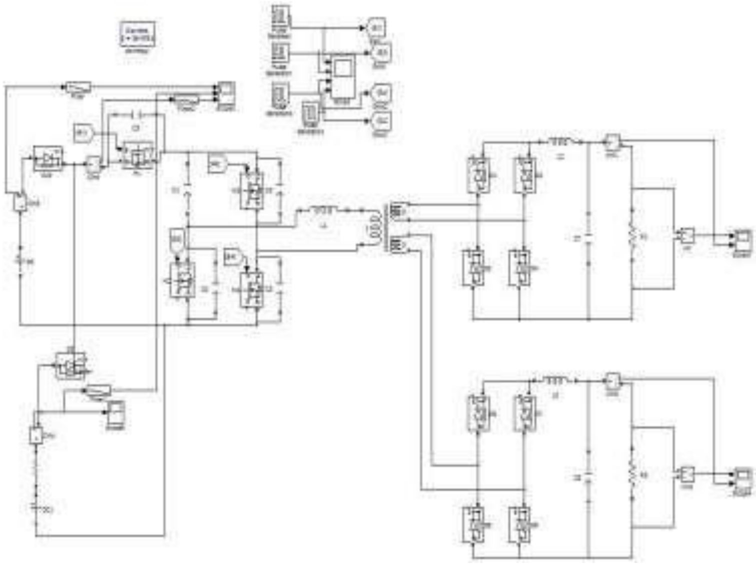

Fig.4.Parallel operation of dc-dc converter

Fig.4 shows the proposed converter. The structure of the transformer primary side is the same as that of the secondary side of the transformer remains the same as the conventional FB or PS-PWM converter. The output capacitances and body diodes of the switches, *S*1 *S*4 respectively. Figure shows key waveforms of the proposed converter. The two gate signals of switches *S*1 and *S*3 (or *S*2 and *S*4) are complementary with the finite dead time, and *S*1 and *S*2 are phase-shifted by 180° same as the double step-down converter.

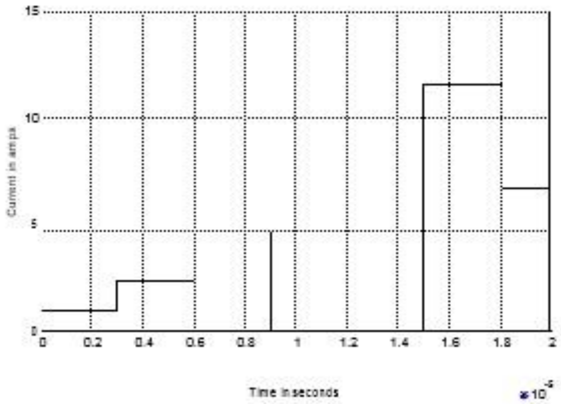

Fig.5 Input current

The Fig.5 shows the input current waveform of the converter .Due to the extended ZVS range of the proposed converter, there is a noticeable difference in efficiency at light Load. Since the conventional converter loses ZVS operation around 1.3 kW, there is relatively sharp efficiency drop at this power level. The proposed converter has slightly lower efficiency at heavy load. This is caused by the higher transformer current and hence higher switch currents and conduction loss. As shown in Figure with the addition of DC-blocking capacitor light load efficiency of the conventional PS-PWM converter becomes slightly lower than that of without DC-blocking capacitor. This is because the addition of DC-blocking capacitor causes lower transformer current, which results in lower available energy for ZVS.

4In this paper, the proposed and conventional PS-PWM converters are tested with the full-bridge rectifier circuits at the secondary sides. However, for this low output voltage the center-tapped rectifier can replace the full-bridge rectifier to further improve the efficiency of both the converters.

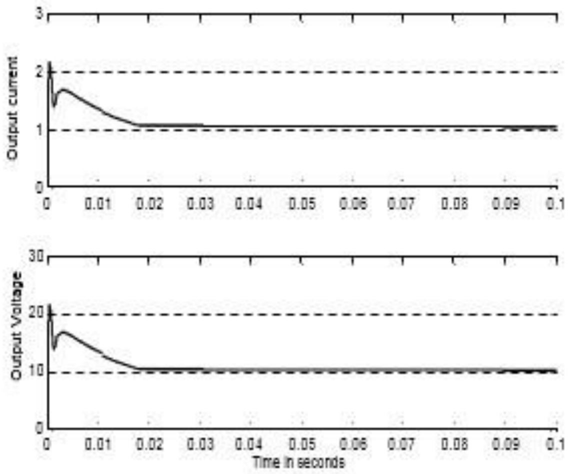

Fig.6 Output voltage of proposed converter

The fig.6 shows the stepped down voltage of the converter. Here double step down operation is performed thus achieving maximum efficiency from the converter output. From the simulation result, we can know that in motoring operation the output voltage increases from zero and reaches the steady state value.

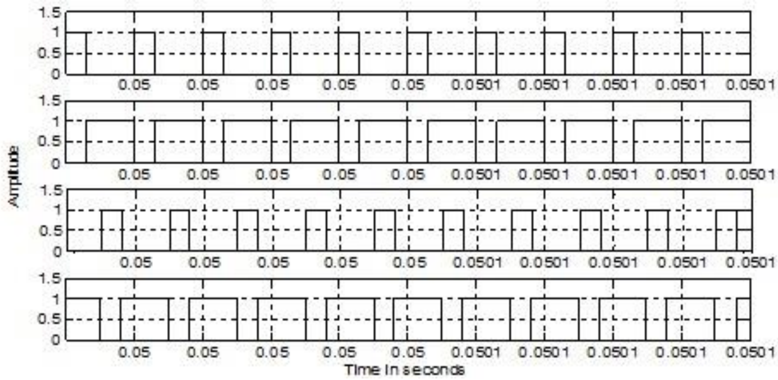

Fig.7 Load voltage and load current

Fig.7 shows the both load voltage and load current waveform. Here voltage is being stepped down to 12 V from an input of 100V.

ISSN: 2459-425X • Website: www.ijrstms.com

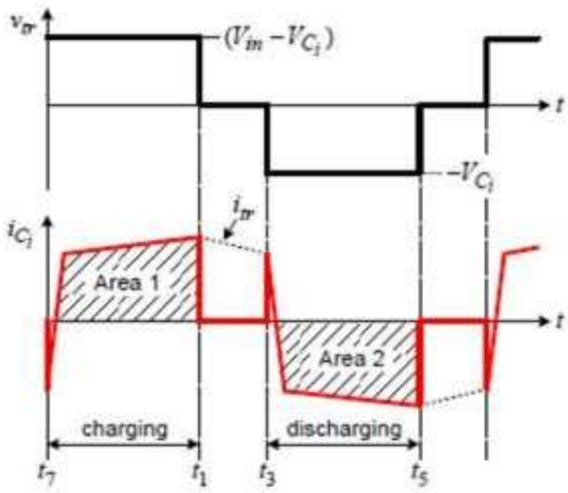

Fig.7 Removal of transformer saturation

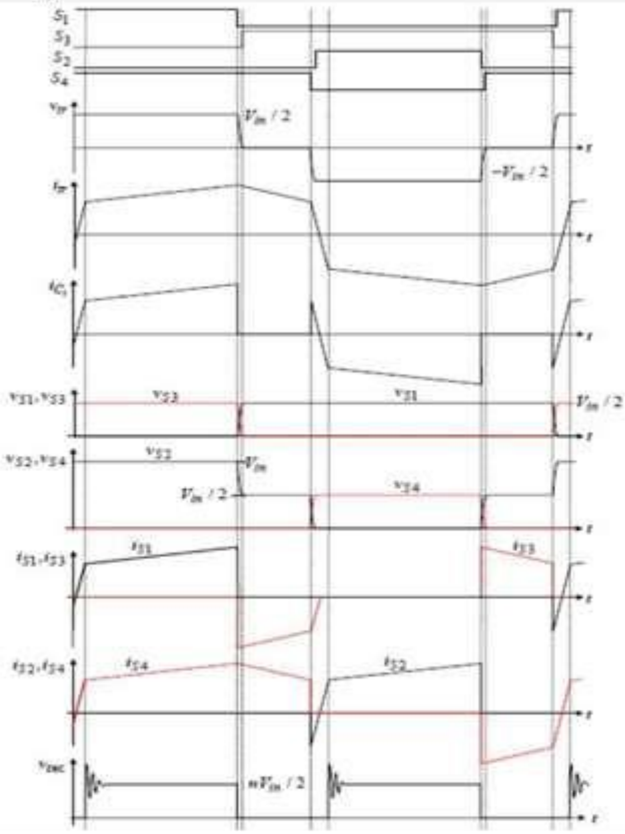

Fig.9 Key waveform of proposed converter

Fig.8 shows the key voltage and current waveform of the proposed converter. The double step down waveform is depicted above

ISSN: 2459-425X • Website: www.ijrstms.com

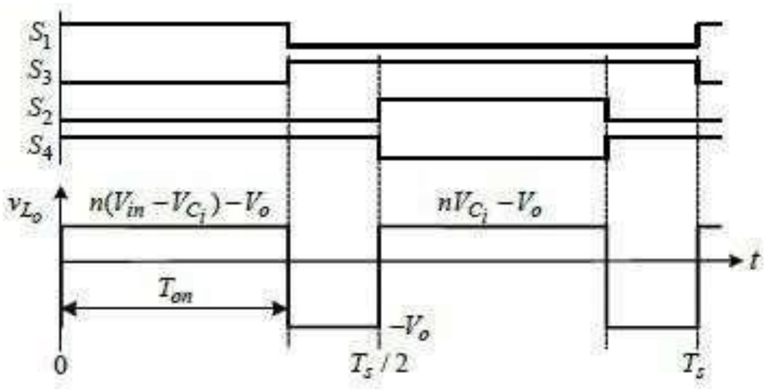

Fig.10 Output Inductor Voltage waveform

From the fig10 shows the output inductor voltage waveform from the MATLAB Simulink output. The relationships between the capacitor *Ci* voltage and input voltage and voltage gain of the proposed converter can be derived from the flux (volt-sec) balance condition on the output filter inductor.

In order to compare the ZVS range, can be used in both converters. As mentioned above, although the proposed converter has to charge/discharge three rather than two capacitors at the same time with the same energy stored in

TABLE I. COMPARISON OF ZVS CONDITION

	Conventional PS-PWM converter	Proposed converter
No. of capacitors charged/discharged	2	3
Switch voltage transition	V_{in} to zero	$V_{in}/2$ to zero
$\frac{1}{2}CV^2$	$\frac{1}{2}(2C)V_{in}^2 = CV_{in}^2$	$\frac{1}{2}(3C)\left(\frac{V_{in}}{2}\right)^2 = \frac{3}{8}CV_{in}^2$
Energy stored in L_{lk}	same	

III. CONCLUSION

In this paper Parallel operation of double step down dc-dc converter, we can conclude that the output voltage has no ripples. Less number of MOSFET switches are used in the converter and the switching loss is minimized. Parallel operation is being employed. The energy stored in capacitor is of compact in size. If one converter got damaged the process is continuous with other one. Voltage stress in minimized in the primary side of transformer. 7

REFERENCES

a) *Angeline Jayachandran, Lakshmi G.R.P.2014 "Analysis and Implementation of Efficient of Drive with Different Converter Systems", IJESRT, ISSN 2277-9655, pp. 2034-2040.*

b) *Clement Mayet, Julien Pouget, Alian Bouscayrol, Walter Lhomme. 2014 "Influence of an Energy Storage System on the Energy Consumption", "IEEE Transactions on Vehicular technology",Vol 63,No.3,pp.1032-1070.*

c) *Chen, X. Yao L., Jiang W., and Hu R. 2015 "A Step-up Converter for Grid-Connected Renewable Energy Source," Power Electronics, IEEE Transactions on, vol. 30, no. 6, pp. 3017-3029.*

d) *Das, P, Pahlevaninezhad M., and Kumar Singh M. 2015 "A Novel Load Adaptive ZVS Auxiliary Circuit for PWM Three-Level DCDC Converters," Power Electronics, IEEE Transactions on, vol. 30, no. 4, pp. 2108-2126.*

e) *Florian Krishmer , Johann Kolar W. 2010 " Accurate Power Loss Model derivation of a High-Current Dual Active Bridge Converter for an Automotive application "IEEE Transactions on Industrial Electronics".Vol.57,No.3, pp.881- 891.*

f) *Juan P. Torreglosa, Pablo Garcia, Luis Fernandz M., Fransico J. 2014 "Improved ZVS PWM three level converter","IEEE Transactions on Industrial Informatics",Vol 10,No.1,pp. 276-285.*

g) *Ming-Shi Huang, Po-Yi Yeh, Jia Rong Huang, Chang-Huang Liao. 2012 "Novel Bidirectional AC-DC Converter for Electrical Testing", IECON, pp.1480-85.*

h) *Saravanan D., Puttalakshmi G.R. 2012 "A Voltage Controlled PFC Boost Converter Fed Drive", IJESRT, ISSN 2277-9655, pp. 890-893.*

i) *Shigenori Inoue, Hirofumi Akagi. 2007"DC-DC Converter for an Energy Storage System for ZVS ","IEEE Transactions on Power Electronics", Vol 22, No.6, pp 2299-2306.*