Design Reduction and Memristor based Logic for Three-Dimensional Pipeline ADC with TSV

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ABSTRACT

High-performance, low-power-consumption, and high-accuracy analog-to-digital converters (ADCs) with a compact area are necessary for a wide range of current applications. This paper presents pipeline ADC architecture with a novel 3-D clock distribution network utilizing through-silicon via-induced benefits. It also implements memristor based logic as the basic elements of digital error correction sub-block to further decrease the area, delay, and power consumption. In addition, an optimization technique using computational intelligence is applied to maximize the overall system performance. The proposed 3-D pipeline ADC is designed in a 65-nm CMOS technology and shows significant improvement regarding dynamic performance, energy efficiency, area, and clock accuracy compared with that of conventional 2-D ADC designs.

KEYWORDS-- 3-D integrated circuits (ICs), clock distribution network (CDN), data converter, evolutionary algorithm, memristor ratioed logic (MRL), performance optimization, pipeline analog-to-digital converter (ADC), and through-silicon via (TSV).

I. INTRODUCTION

The continuous scaling of advanced CMOS technologies makes interconnection a key limiting factor in latency and power/area efficiency. The 3-D integrated circuits (ICs) can be a promising solution that overcomes the technical barriers in high-performance communication systems by using their capabilities of chip area reduction, signal integrity and less routing complexity. Recently, some analog/mixed-signal IC prototypes have explored 3-D design advantages in areas such as stacked memory chips, memories on CPU, co-integration of antenna and RF micro-electromechanical systems and image sensor layer stacking on the memory and CPU layer. However, 3-D analog-to-digital converter (ADC) design has not been studied because of their complicated structure compared to the other mixed-signal IC prototypes.

In a 2-D ADC design, one of the major challenges is routing congestion on the die leading to increased latency and degraded signal integrity due to long metal interconnections. The conventional ADC prototype has the lack of analysis on inherent key design challenges such as clock distribution network (CDN) latency, power overhead, and on-chip routing complexity. Thus, a considerable amount of research concerning CDN has already been carried out to reduce the skew and jitter in 2-D ICs. Many 2-D CDN topologies such as trees and grids have already been proposed.

Pipeline ADCs implement a large number of critical clock phases (i.e., non overlapping sampling clocks, multiplier DAC (MDAC) clock, and sub-ADC clock) to synchronize all gain stages (GSs). Hence, when the clock signal paths to each GS are symmetry, the clock skew is minimized in ADC design. Some techniques such as H-tree and X-tree can provide the clock distributions symmetry. However, they cause more design complexity, power consumption, and area overhead.

In a pipeline ADC with unsynchronized sampling clocks, the jitter and noise reduce signal to noise ratio (SNDR), introduce spurious emissions, and thereby further limit the spurious-free dynamic range (SFDR). Thus, the key performance parameters such as SNDR and SFDR can become critical limitations of sampling accuracy when the routing length and complexity increase. While the SNDR depends on various factors, the effect of broadband jitter on the clock signal is given as follows:

$$SNDR_{JITTER} = -20 \log 10(2\pi f_{IN} \times T_{JITTER}) \quad (1)$$

Where, fIN is the input frequency and TJITTER is the jitter in RMS. Fig. 1(a) shows a long and complex on-chip clock routing in a conventional pipeline ADC. Since the clock signal is a sampling time reference in all GSs, it has to be distributed throughout the die using metal interconnects. As a consequent, for a high-resolution pipeline ADC, the clock delay and skew/jitter to the GSs that must be accurately synchronized, increases relatively, as shown by the red solid line in Fig. 1(b). The created clock skew/jitter can directly affect the maximum converter speed. However, the proposed 3-D ADC can significantly decrease the clock jitter which is often dominated by the white noise floor of the clock signal.

In addition to the 3-D implementation, memristive devices can further extend the capabilities of ADC performance. The memristor can be described as a two-port passive element with variable resistance (memristance). Fig. 1(c) shows the memristor symbol, model, and key characteristics of the current–voltage curve. The thick black line on the symbol shows the negative polarity of the memristor. When the current flows from the negative to the positive polarity, the memristance increases and follows the ROFF line on the curve; while in the positive to the negative polarity of the current flow, the memristance decreases and follows the RON line on the curve. In this paper, a hybrid CMOS-memristor logic family, namely, memristor ratioed logic (MRL), has been utilized in the digital blocks of the pipeline ADC to decrease the clock delay further and increase the logic density. By incorporating the MRL into the proposed 3-D ADC, we can also decrease the power consumption, interconnection complexity, and parasitic capacitance.

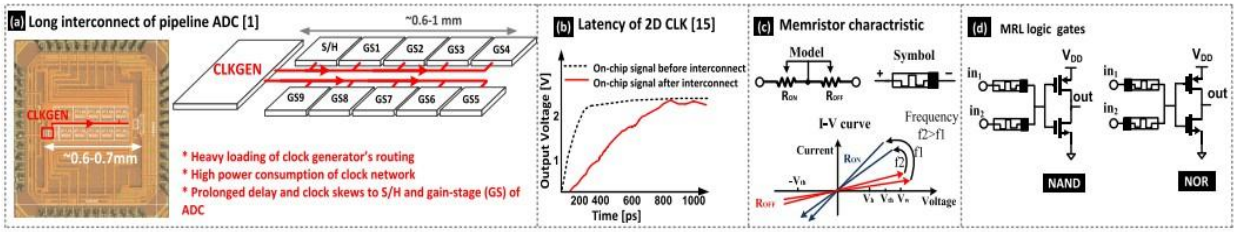

Fig. 1. (a) Conventional 2-D pipeline ADC with considerable power consumption, clock delay, and heavy clock loading. (b) Sample 2-D clock after passing through the on-chip track. (c) Memristor symbol, model, and characteristic. (d) MRL logic basic elements.

Fig. 1(d) shows the MRL basic logic gates. In MRL, OR, and AND logic gates are based on memristors, and CMOS inverters are added to improve the logic function and create the output signal restoration. Both OR and AND logic gates are composed of two series connected memristors that have opposite polarity. MRL occupies 67.6% and 75% less silicon area in NAND and NOR logic configurations, respectively. As a result, the propagation delay for a full adder, utilizing the MRL-based logic gates, can be decreased about 30% which can improve speed of the ADC digital subblocks. Therefore, we have a less number of transistors on the chip for the same functionality to improve the speed, decrease power consumption, and save the die area.

This paper analyzes and presents a novel ADC design exploiting 3-D CDN, MRL logic, and computational intelligence. The proposed scheme is designed and analyzed on a 10-bit pipeline ADC as a prototype because the pipelined architecture has most successfully fulfilled the features of advanced CMOS technologies. Utilizing a hierarchical block-based evolutionary algorithm has maximized the overall ADC performance such as dynamic specifications, power, accuracy, and area. To the best of the author's knowledge, the proposed 3-D pipeline ADC

design in which MRL logic and evolutionary algorithm are incorporated to obtain the optimal design point and intertier routing has never been investigated. Although the proposed MRL/3-D integration approach looks to arouse extensive interest of industry and academia and have a promising contribution to future high-speed ADC generation, the manufacturing technology is not that much common and easy access, yet. Thus, commercially memristors are not expected to be available in the near future. The rest of this paper is organized as follows. Section II discusses the proposed 3-D ADC design architecture and presents the implemented through-silicon via TSV)/wire model and MRL logic. The evolutionary approach is discussed in Section III to find the optimal transistor sizing and TSV geometry. Section IV shows the simulation and evaluated results. Finally, the conclusion is given in Section V.

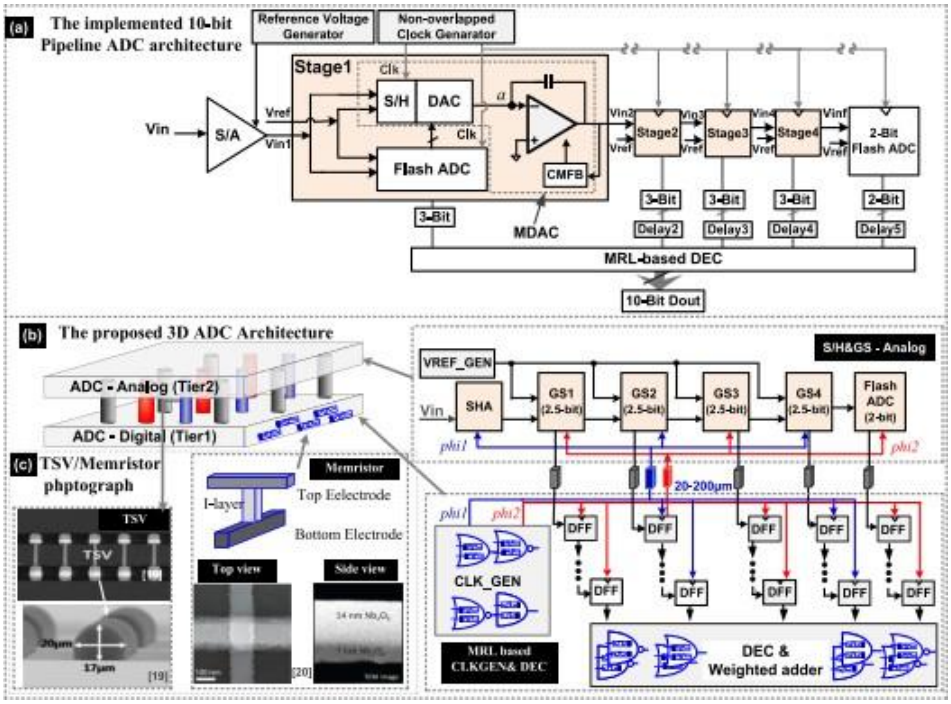

Fig. 2. (a) Implemented 10-bit pipeline ADC conceptual diagram.(b) Proposed 3-D pipeline ADC architecture. (c) TSV channel and memristor microphotographs.

II. ARCHITECTURE CONSIDERATIONS

Fig. 2(a) shows the 10-bit pipeline architecture considered for 3-D implementation. This architecture is composed of a sample and hold (S/H) block, four 2.5-bit GSs followed by a 2-bit back-end flash ADC and digital error correction (DEC) block. In pipeline ADC design, back-end GSs sizing can be scaled down to reduce their input-referred noise. However, preceding work has illustrated that for a 10-bit pipeline ADC, the current structure has the minimum power consumption and input-referred noise. Thus, the pipeline structure, shown in Fig. 2(a), has been employed. Fig. 2(b) shows the proposed 3-D pipeline ADC architecture by placing analog and MRL-based digital circuits into the top and bottom tiers, respectively. This architecture can significantly improve the critical clock synchronization and deskewing in highresolution pipeline ADCs by fully utilizing the advantage of vertically short TSV channels.

It also considerably reduces the design complexity and increases the accuracy due to the suppression of the intertier clock skew/latency and improved clock synchronization. Fig. 2(c) shows the physical structure and microphotographs of TSV channels, μbumps, and memristors (i.e., side view and top view).

Fig. 3 illustrates in detail how the clock jitter and timing skew can significantly affect the conversion accuracy in a high speed pipeline ADC. Fig. 3(a) and (b) shows different clocks of each subblock inside a 1.5-bit GS and their switching timing priority, respectively. Since in a pipeline ADC regeneration nodes [i.e., a in Fig. 2(a)] are inherently coupled to the input of the comparator through the transistor parasitic capacitances, this coupled voltage, known as kickback noise, can disturb the input signal and result in the error at the outputs.

Fig. 3(c) depicts a conventional approach to reduce the kickback noise effect on each GS of the pipeline ADC and also generate two non-overlapping conversion phases. The tracking phase of the comparator (*phi* COMP*)* is delayed with respect to the phase (*phi1a*) to prevent their coincidence at the regeneration node. However, this time interval and also the non-overlapping timing period of two basic conversion phases (i.e., *phi1* and *phi2*) can be degraded when the CDN length becomes longer. Therefore, by considering the proposed 3-D CDN-based ADC, utilizing the TSV channels, delay skew between *phi1a* and *phi* COMP can be significantly reduced, and thereby the kickback noise further decreases. It also can maintain more precise two non-overlapping pipelined conversions. The following describes the implemented models of TSV and wire for the 3-D CDN-based pipeline ADC.

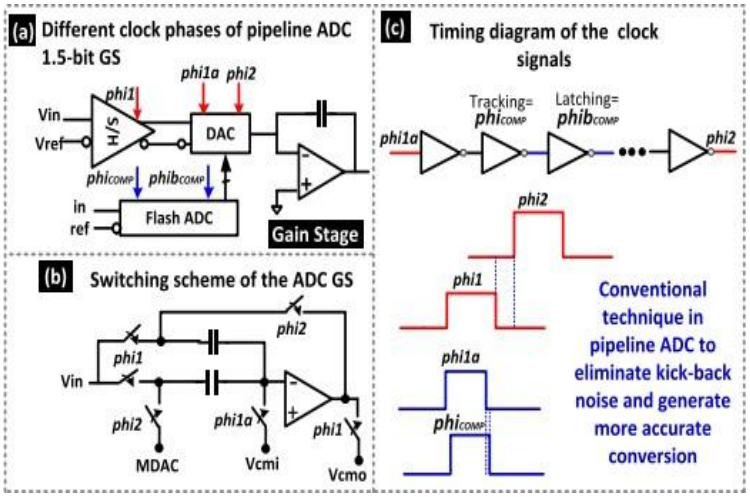

Fig. 3. Delayed tracking time scheme of the pipeline ADC clocks for TSVs. preventing kickback noise and clock skew.
(a) Different clock phases Of pipeline ADC.
(b) Timing diagram of the clock signals.
(c) Switching scheme of the ADC GS.

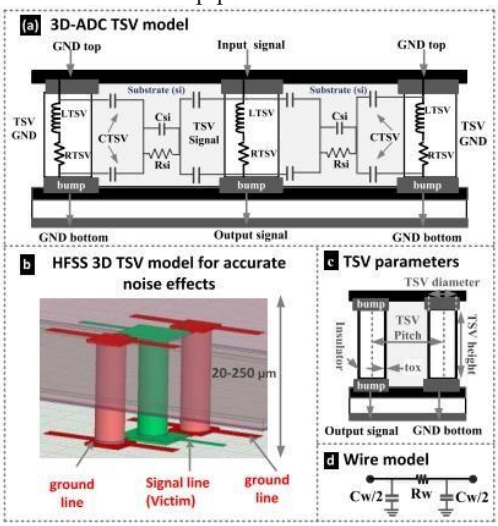

Fig4(a) Modeling of coupling effect between
(b) HFSS model.
(c) TSV design parameters.(d) Wire model.

A. TSV Model for 3-D ADC Design

The electrical model and design parameters of the signal/ground TSVs are illustrated in Fig. 4(a). This model shows one signal TSV surrounded by two ground TSVs with *µbumps* inside the silicon substrate. The ground TSVs can provide a shielding for the signal TSV and make the 3-D routing signal integrity less noise sensitive. The 3-D channel includes TSV as well as *µbumps*. The scalable electrical lumped model is simulated by a 3-D electromagnetic simulator such as HFSS, as shown in Fig. 4(b). The TSV model includes coupling effect between two adjacent TSVs that can degrade the 3-D channel signal integrity. Each TSV is surrounded by a layer for isolating the TSV from the conductive silicon substrate. This model also considers other parasitic effects between the *µbump* and the silicon substrate in the intermetal dielectric (IMD), *µbump* capacitors and bottom oxide layer capacitor. The analytic equations are derived from the physical configuration including the design parameters. The TSV resistance is also analytically formulated from the geometric parameters. As the frequency increases, the current flows on the surface of the TSVs. Dependence to the frequency is measured by the skin depth. The TSV inductance is modeled with a calculation to the "two-wire interconnection line model" The silicon resistance *R*si and capacitance *C*si have been also considered as two optimization parameters. The evolutionary parameters are shown in Fig. 4(c) where *h*TSV, *d*TSV, *t*ox, and *P*TSV are TSV height, TSV diameter, insulator thickness, and the pitch between two TSVs, respectively. Moreover, ρTSV, $\mu 0$, $\varepsilon 0$, μr, and εr,IMD represent TSV electrical resistivity, magnetic constant, electrical constant, relative magnetic and electrical permeability of IMD layer, respectively. The TSV design parameters such as capacitance and resistance can be affected by the *d*TSV, *h*TSV, and *P*TSV. Therefore, a computational intelligence-based optimization by using the TSV design parameters is performed, and the optimal tradeoffs between power, latency and signal integrity is achieved.

B. Wire Model for 3-D ADC

The latency and power consumption optimization in a 3-D design needs wire *RC* estimation and improvement in addition to the TSV optimization. To estimate wire parameters, the metal layers, assigned for

interblock signals, must be defined, i.e., M4–M6 layers are the commonly used. Considering copper as the wire material, the relevant *RC* values [i.e., Fig. 4(d)], as well as TSV coupling capacitance with adjacent wires, are estimated using the Wu–Wong model.

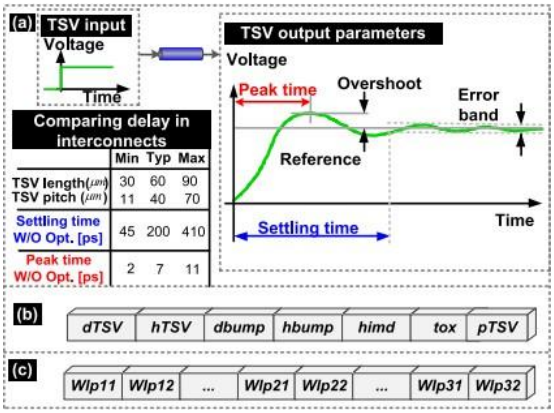

Fig. 5. (a) Time corresponding performances of the TSV fitness function.(b) TSV and (c) ADC subblock evolutionary design parameters in a GA chromosome string

III. EVOLUTIONARY PROCESS OF TSV AND SUBBLOCKS

To achieve the best performance and power/area efficiency, the proposed 3-D CDN-based design utilizes an evolutionary method by considering all design parameters (i.e., ADC transistor sizing, CDN design parameters, and TSV model variables such as width, height, and pitch) concurrently. In this novel co-optimization, the key TSV geometry model and circuit design parameters of the 3-D pipeline ADC are individually defined as the input variable vectors in MATLAB. A kind of MATLAB-HSPICE toolbox interface is created to simulate the proposed CDN-based ADC utilizing genetic algorithm (GA) as the evolutionary solver. After each HSPICE simulation, MATLAB links to HSPICE to evaluate desired performance parameters and feed the new design points to GA.

To the best of our knowledge and based on the references, the simultaneous optimization of 3-D ADC/CDN design and TSV geometry is first reported in this paper; although there are some works on ADC design and TSV model optimization. In this co-optimization *of* 3-D pipeline ADC design and TSV geometry, different performance parameters conflict with one another (i.e., signal integrity and coupling effect parameters of TSVs, and latency and power parameters for ADC). Thus, the optimization problem requests tradeoffs that would compromise a general synthesis computational efficiency. These tradeoffs are called as *Pareto fronts* in computational intelligence to find the optimum design points.

A. Evolutionary Process of TSV

Fig. 5(a) shows the performance parameters of the TSV optimization. Given an *n*-dimensional decision variable vector $x = \{x1, \ldots, xn\}$ in the solution space *X* (i.e., *X* represents the whole design parameter space), the TSV optimization problem can be formulated as to find a vector $x*$ that minimizes a set of *K* objective functions $z(x*) = \{z1(x*), \ldots, zk(x*)\}$. The solution space *X* is generally restricted by a set of equality constraints denoted by $g\,j(x*) = b\,j$ for $j = 1, \ldots, m$, and bounds on the decision variables. The GA tries to obtain all TSV sizing parameters through a reduced set of independent variables, namely, gene. These variables shape the chromosome string. The corresponding string is shown in Fig. 5(b) where *d*bump, *h*bump, and *h*imd represent *μbumps* diameter, *μbumps* height, and IMD height, respectively. The GA's fitness function, shown in (2), at the bottom of this page, including all TSV output signal specification finds the optimum design parameter of TSV. For example, the better fitness function has lower settling time, error band, overshoot percentage, peak time, and higher peak absolute value.

B. Evolutionary Process of ADC Sub-blocks

To improve the overall performance of the 3-D ADC, it is necessary to attain the optimal subblock design points and the scaling factor of GSs by utilizing the optimal TSV geometry obtained from the first evolutionary process. To improve the efficiency and minimize search space, a hierarchical multiobjective optimization is implemented.

Fig. 5(c) shows an example of each subblock chromosomein the evolutionary process; where *WLp*11 and*WLp*12 show transistors width(*W)* to length (*L)* ratio inside each analog subblock and *p* represents the transistor pair number. The best (minimum) fitness function value can be obtained using

$$\text{fitness\_function} = -\frac{k_0 \times \text{SNDR} + k_1 \times (\text{FOM})^{-1}}{k_2 \times \text{Power} + k_3 \times \text{Area}}. \quad (3)$$

Since dynamic performances improve the ADC applicability and give a better understanding of its most critical parameters such as linearity and spectral purity, SNDR is the most effective term of the fitness function. Higher SNDR can also improve the bit rate. Thus, the relevant coefficient $k0$ is chosen so that the SNDR term in the numerator (3) is several times more effective than others. The second key factor is figure of merit (FoM), with coefficient $k1$, and consists of total circuit power consumption Pw sampling frequency fs and effective number of bits (ENOB)

$$\text{FOM} = \frac{Pw}{2^{\text{ENOB}} \times f_s}. \quad (4)$$

The third significant parameter that GA tries to minimize is power consumption. In (3), $k2$ changes the effect of power consumption on the fitness value. Since a high-speed pipelined ADC power consumption is mostly dominated by the analog blocks, the evolutionary process tries to minimize this portion of the power consumption. The silicon area minimization is the last effective factor, extracted from the applied elements sizing. Thus, $k3$ is assigned in a way to have the least impact on fitness function compared to the other terms.

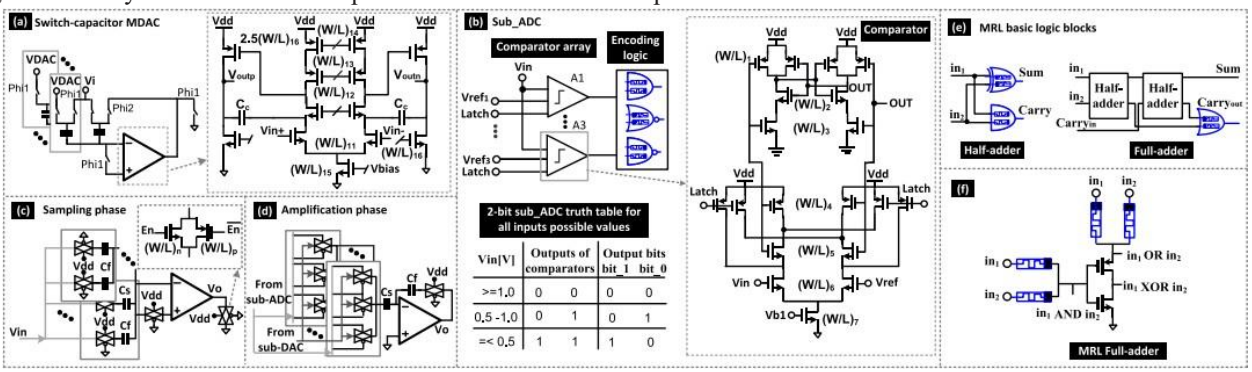

Fig. 6. (a) Switch-capacitor scheme, inside the applied 2.5-bit stages and MDAC circuits. (b) Sub-ADC and all possible input signal Vin values and their corresponding output digital codes. (c) Sampling and (d) amplification phases using transmission gate (TG) switches. (e) Schematic of the MRL-based half and full adder, using two-input NAND/NOR gates. (f) Full-adder MRL-based implemented in the DEC block.

IV. SIMULATION RESULTS

The proposed architecture described in Section II was implemented on a 10-bit pipeline ADC at 120 MS/s in 65-nm technology with a 1-V power supply. The circuit simulations are performed by using Spectre simulator and HSPICE-MATLAB interface in MATLAB R2016a environment. To evaluate the performance accurately, the postlayout extracted simulation was performed by considering the parasitic resistance and capacitance of the 3-D ADC design. Fig. 6 shows the schemes of the optimized ADC subblocks as the case study. The switch-capacitor MDAC is shown in Fig. 6(a). To have a fast output settling time, low-voltage operation, and high-gain amplifier, a two-stage telescopic cascade topology is implemented. For improved stability and phase margin, a Miller compensation scheme is utilized in the GS amplifier. Fig. 6(b) shows the sub-ADC block generates three coarse output bits from the input signal (Vin). A comparator latch is also utilized to synchronize further any potential clock skews from the 3-D CDN. Fig. 6(c) and (d) shows the operation of a multiplier MDAC (MDAC) utilizing transmission gate (TG) switches in signal sampling and amplification phases, respectively.

Fig. 6(e) and (f) shows the schematic of the MRL-based half and full adder, using two-input NAND/NOR gates, implemented in the DEC block. As it was pointed out, both logic NAND and NOR gates consist of two memristive devices where their polarity is the only structural difference. Since the memristor voltage divider degrades the output voltage (i.e., ROFF RON), CMOS inverter is integrated into an MRL OR/AND logic gates to improve the output voltage. However, the delay time of the logic gates changes with capacitance of the CMOS gate and consequently needs optimization.

As illustrated in Fig. 6(a), the GS introduces seven design variables which consist of six transistor sizes and one Miller capacitor value. Using equal size transistors for the implemented switches (transmission gates) adds a new evolutionary variable. The comparator transistor sizing also introduces seven new variables, as shown in Fig. 6(b). A total of 14 variables can be used as a chromosome vector by the evolutionary algorithm leading to a fast and accurate performance optimization.

The fitness function of the pipeline ADC is constrained to give at least eight-effective bit resolution at the Nyquist rate. When the proposed co-optimization algorithm is used to a 10-bit pipeline ADC, the acceptable solutions in each iteration should have SNDR more than 49.9 dB using a 1024-point fast Fourier transform. Fig. 7 shows the improvement of the TSV channel performance parameters such as latency, power consumption, and output voltage overshooting utilizing the evolutionary process on TSV over 100 iterations. Power simulations are performed based on the power consumption per TSV in a 3 × 4 TSV array. Before the evolutionary process, the 3 × 4 TSV array generates 0.35-μW average power. As expected, the TSV latency (i.e., from 25 ps to sub-1 ps), I/O power per channel (i.e., from 45 to 21 μW), and output voltage overshooting (i.e., from 0.8 to 0.05 V) are minimized after the evolutionary process. Diagrams of the multiobjective optimization process to explore the tradeoffs between power consumption and latency of the proposed 3-D ADC, considering the optimized TSVs, are shown in Fig. 8. Based on the trend of the Pareto-front plot, we can evaluate the most optimal design point for a highperformance and low-power 3-D ADC architecture.

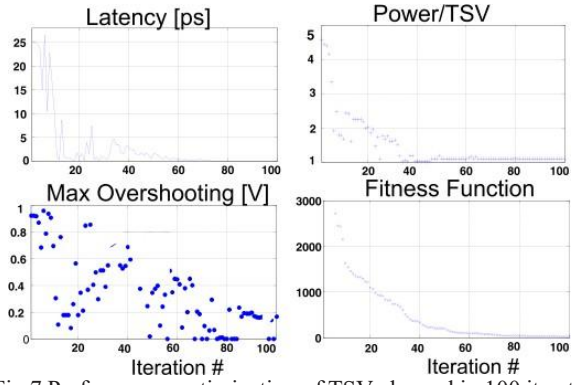

Fig.7 Performance optimization of TSV channel in 100 iterations.

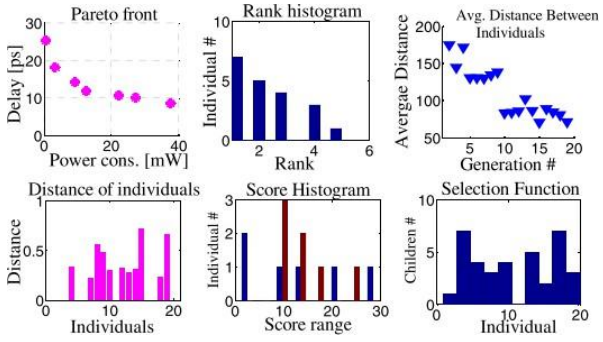

Fig.8.Multiobjective evolutionary process of the proposed ADC.

Table I shows a summary of the optimization parameters. By utilizing the multi-objective hierarchical optimization, the computational overhead is reduced because of limiting the search space. Table I shows the entire design cycle took about 3 h on a high-performance computing server with 128-GB RAM 16-core Intel(R) Xeon(R) CPU X5560 at 2.80-GHz 107 processor.

TABLE I

EVOLUTIONARY SPECIFICATIONS OF THE PROPOSED ALGORITHM

NO. of variables	Population size	Generation No.	Crossover	Mutation probability	Stopping condition	Total performance improvement(%)	Total convergence time (hr.)
15	40	20	Scattered	0.05	Stall generation	23	3

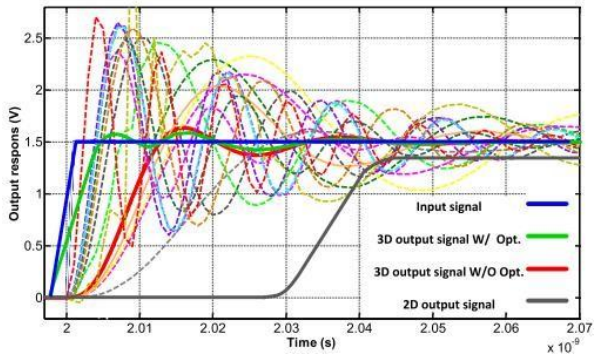

Fig. 9. Evolution of 3-D TSV output signal

Fig. 9 shows the final TSV channel output waveforms by considering the TSV/ADC subblock design parameters and MRL logic. As expected, the optimized output voltage is significantly improved regarding delay, power, and overshooting with the obtained design parameters. The dotted lines show the final ADC output voltage waveform after each iteration. Green and red lines show the ADC output voltage waveform with and without optimization, respectively. The black line shows the CDN output voltage signal in a 2-D pipeline ADC.

To verify performance improvement of the proposed 3-D ADC design versus 2-D conventional design, we also implemented Fig. 10(a) and (b) show the ADC output power spectrum for 2-D and 3-D designs, respectively. As predicted, the proposed CDN-based 3-D ADC design utilizing the co-optimization methodology results in significant improvement of the performance [i.e., SNDR increased from 53.11 dB (2-D) to 59.88 dB (3-D/w MRL and optimization)]. Fig. 11 shows the power consumption and the signal delay of each investigated case (i.e., the conventional 2-D ADC, 3-D ADC using MRL logic with and without the optimization).

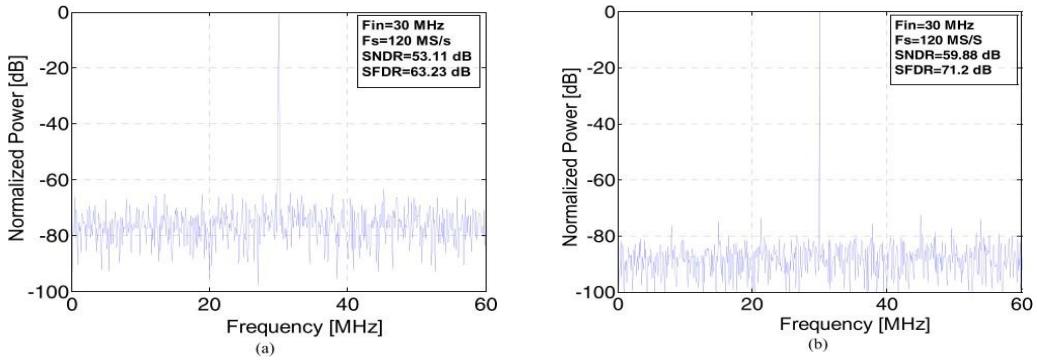

Fig. 10. ADC power spectrum using (a) conventional 2-D design and (b) proposed 3-D ADC design.

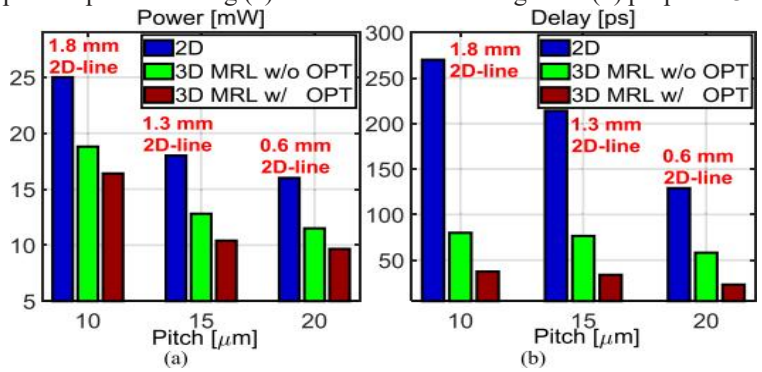

Fig. 11. Two-dimensional versus nonoptimized/optimized 3-D ADC using MRL logic (a) power consumption and (b) clock delay for different TSV placements and interconnection line length with 60-μm TSV height.

Fig. 11 shows the signal delay has significantly decreased by considering the TSV vertical connections instead of 2-D long interconnections. It also shows that the proposed 3-D ADC utilizing the co-optimization algorithm as well as MRL logic can improve power efficiency compared with 2-D design. Moreover, as the TSV pitch decreases, the power consumption can be increased dramatically (i.e., from 19 to 12 mW). Table II compares the performance of the state-of-art pipeline ADCs and the proposed 3-D ADC.

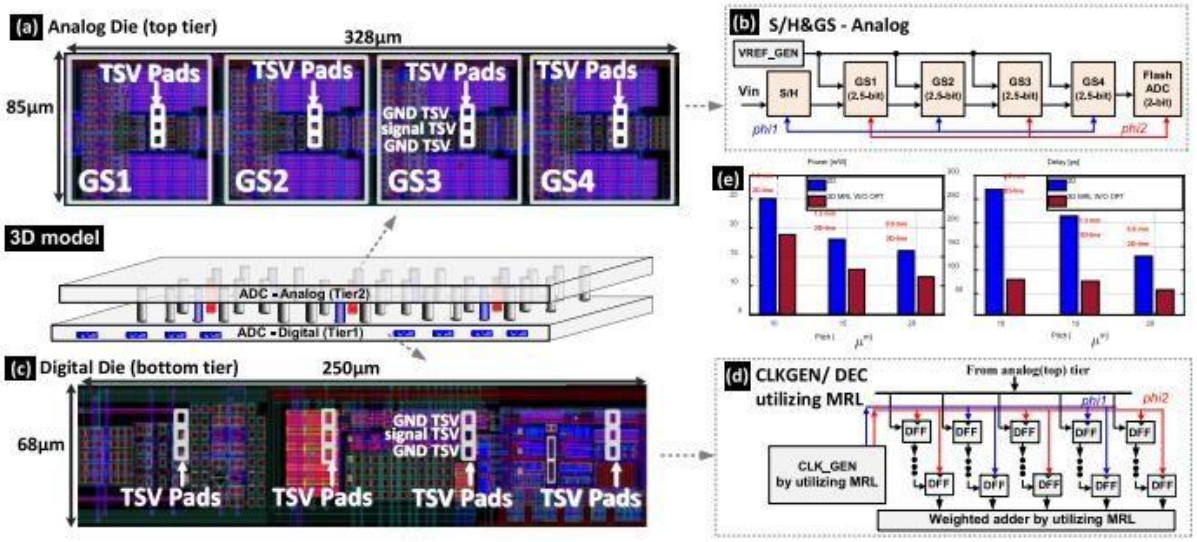

Fig. 12. (a) Analog/top die layout and (b) scheme. (c) Digital/bottom tier layout and (d) scheme of the 3-D pipeline ADC. (e) Comparison bar diagrams for the ADC power and signal delay.

As summarized in Table II, in an identical technology, this design can achieve considerably less power consumption than other techniques which implement particular power saving policies such as amplifier sharing, sample and hold less design or switched amplifier methods.

Moreover, a higher performance specification has been achieved and determined after considering both evolutionary process and MRL architecture (i.e., SNDR is increased from 57.3 to 59.9 dB). In addition, implementing TSV-aware optimization and MRL logic has reduced FoM up to 37%.

The results confirm that the proposed 3-D design algorithm searches for a circuit with higher conversion accuracy and lower power dissipation, while other parameters such as SNDR and FOM are improved at the same time. Fig. 12 shows the 3-D pipeline ADC layout and block diagrams of analog and digital tiers, implemented in the 3-D simulation. It also shows the power and delay bar diagrams that compare 2-D with 3-D ADC simulation results.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	Previous works			This work	
	TVLSI 15 [33]*	TCASI 16 [34]*	JSSCC 15 [35]*	3D	3D MRL /w Opt.
Bit #	10	14	12	10	10
Supply [V]	1.2	1.8	1	1	1
Tech. [nm]	130	180	40	65	65
Sample rate [MHz]	200	250	195	120	120
SFDR [dB]	63	87	82	68.7	71.2
SNDR[dB]	53	68	64.8	57.3	59.9
Power[mW]	38	300	53	11.4	9.6
FOM [fJ / Conv.]	552	570	157	158	98.8

(* Measurement results)

V. CONCLUSION

This paper presented a 3-D pipeline ADC design with a novel CDN architecture by utilizing 3-D channel and MRL to improve the conversion accuracy, dynamic performance, and power/area efficiency. In addition to implementing MRL digital blocks, implementing a multiobjective evolutionary algorithm on the analog blocks of the proposed 3-D ADC has further provided the overall performance improvement regarding power, delay, and area efficiency. The prototype pipelined ADC achieves 59.9 dB SNDR at 120 MS/s with 9.6-mW power consumption. It also has a 98.8 fJ/conversion step, which shows a significant improvement among the designs compared.

REFERENCES

[1] Y. Lim and P. F. Flynn, "A 100 MS/s, 10.5 bit, 2.46 mW comparatorless pipeline ADC using self-biased ring amplifiers," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2331–2341, Oct. 2015.
[2] J. Knechtel, I. L. Markov, and J. Lienig, "Assembling 2-D blocks into 3-D chips," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 31, no. 2, pp. 228–241, Feb. 2012.
[3] D. Malta *et al.*, "TSV-last, heterogeneous 3D integration of a SiGe BiCMOS beam former and patch antenna for a W-band phased array radar," in *Proc. IEEE Electron. Compon. Technol. Conf. (ECTC)*, May 2016, pp. 1457–1464.
[4] W. Liu, G. Chen, X. Han, Y. Wang, Y. Xe, and H. Yang, "Design methodologies for 3D mixed signal integrated circuits: A practical 12-bit SAR ADC design case," in *Proc. IEEE Int. Symp. Quality Electr. Design*, Jun. 2014, pp. 1–6.
[5] K. Kim, "Silicon technologies and solutions for the data-driven world ," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–7.
[6] M. M. Shulaker, T. F. Wu, M. M. Sabry, H. Wei, H.-S. P. Wong, and S. Mitra, "Monolithic 3D integration: A path from concept to reality," in *Proc. IEEE Design, Autom. Test Eur. Conf. Exhibit. (DATE)*, Mar. 2015, pp. 1197–1202.
[7] T. Kondo *et al.*, "A 3D stacked CMOS image sensor with 16 Mpixel global-shutter mode and 2Mpixel 10000 fps mode using 4 million interconnections," in *Proc. Symp. VLSI Circuits (VLSI Circuits)*, Jun. 2015, pp. C90–C91.
[8] R. Li, C. Jin, S. C. Ong, T. G. Lim, K. F. Chang, and S. W. Ho, "Embedded wafer level packaging for 77-GHz automotive radar frontend with through silicon via and its 3-D integration," *IEEE Trans. Compon., Packag. Manuf. Technol.*, vol. 3, no. 9, pp. 1481–1488, Sep. 2013.
[9] S. C. Chan *et al.*, "A resonant global clock distribution for the cell broadband engine processor," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 64–72, Jan. 2009.
[10] L. Zhang, A. Carpenter, B. Ciftcioglu, A. Garg, M. Huang, and H. Wu, "Injection-locked clocking: A low-power clock distribution scheme for high-performance microprocessors," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 16, no. 9, pp. 1251–1256, Sep. 2008.